Engineering Journal issn: 0125-8281

Article

FPGA Implementation of Phase Noise Equalization for High Speed 5G OFDM using Parallel Processing Algorithm

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Abstract. Phase noise significantly degrades the system performance in high-speed 5G orthogonal frequency division multiplexing (OFDM) systems, particularly within the challenging FR2 band, which can support up to 400 MHz of bandwidth. As a result, efficient cancellation techniques for phase noise are necessary. This paper introduces an effective field-programmable gate array (FPGA) implementation for phase noise cancellation in 5G OFDM. To address the inherent limitations in FPGA clock speed at high data rates, parallel processing is employed. Additionally, a novel complex multiplication optimization is presented, which significantly reduces logic gate usage and enhances hardware efficiency compared to standard methods. The effectiveness of the proposed maximum likelihood estimation (MLE) based approach is confirmed through simulations and real-time testing on a Virtex-7 FPGA. The results show excellent agreement between simulation and hardware, with significant phase noise reduction and bit error rates (BER) below 10^{-3} for 16-QAM and 64-QAM, and 10^{-2} for 256-QAM. The implementation is highly efficient, using only 3% of FPGA slices, demonstrating its practical feasibility for 5G FR2 deployments.

Keywords: Orthogonal frequency division multiplexing, 5G, phase noise equalization, FPGA.

ENGINEERING JOURNAL Volume 29 Issue 8
Received 14 April 2025
Accepted 21 July 2025
Published 31 August 2025
Online at https://engj.org/
DOI:10.4186/ej.2025.29.8.67

DOI:10.4186/ej.2025.29.8.67

1. Introduction

Mobile communication systems have undergone extensive development in response to the constantly growing demand for faster communication speeds and the connection of a large number of devices per square meter. To meet this requirement, an advanced modulation format is necessary. Orthogonal frequency division multiplexing (OFDM) is widely used in mobile communication systems worldwide. Specifically, according to the standards, the fourth generation (4G) and fifth generation (5G) utilize OFDM as their modulation scheme [1 - 2], and it remains a promising candidate for the sixth generation (6G) shortly [3-4]. Additionally, Wi-Fi 6 and 7 have also adopted OFDM as their standard technologies [5-6]. Over the past decade, non-orthogonal frequency division multiplexing communication systems have been extensively researched, as reported in [7-8]. Unfortunately, these systems are still under development and currently in the testing phase.

OFDM demonstrates high tolerance to intersymbol interference (ISI) by effectively mitigating it through appending its own samples from the end into the front of each OFDM symbol [9]. This part of the process is known as cyclic prefix (CP). For single-carrier communication systems, fading can cause attenuation across the entire frequency spectrum. Unlike OFDM, which is a multi-carrier system, only some subcarriers are affected by fading. Consequently, some subcarriers can be used, but with reduced communication speed [8]. However, all the subcarriers in OFDM must remain orthogonal. Intercarrier interference (ICI) can still occur despite successful resolution of ISI. ICI is primarily caused by two issues: carrier frequency offset (CFO) and phase noise (PN). Both disrupt the orthogonality among subcarriers, resulting in power leakage from one subcarrier to others, which increases the total power sum. This leads to the destruction of both phase and amplitude, degrading system performance [9-10]. Generally, this phenomenon limits the communication speed of OFDM systems. In this work, however, only phase noise, which is an unavoidable factor in practical communication systems, is considered. However, it can be canceled or mitigated. Phase noise is a random fluctuation in phase rotation caused by oscillator imperfections, which prevent a purely single-frequency output. Specifically, sidelobe frequencies close to the primary frequency are also present. The impact of phase noise can be especially severe in millimeter wave communication systems [10-11]. Therefore, the OFDM communication system is critical to mitigate the effect of phase noise to improve and stabilize the performance of 5G systems and beyond.

Numerous approaches have been proposed to mitigate phase noise. Commonly employed techniques include maximum likelihood estimation (MLE) [12] and decision-directed (DD) [13, 15]. The MLE method computes the average phasor rotation from the pilot signal, which involves embedding known data from the transmitter. This process results in some subcarriers being designated for pilots, thereby reducing the effective data rate. The DD method utilizes a feedback loop and iterative calculations of the phasor rotation between preceding and current symbols. Although these algorithms are theoretically well-founded, their implementation in real-time contexts, particularly for high bandwidths such as 400 MHz and the stringent latency requirements of 5G FR2 systems, presents considerable practical challenges. The feedback loop necessary for the iterative process complicates efficient hardware implementation of the DD method in high-speed communication systems, making hardware efficiency critical consideration.

1.1. Related Works

Based on the literature reviews, the FPGA implementation of the phase noise compensation algorithm is rarely found. Perhaps it is a secret of each company and developer that is not allowed to be made public. In [14], the authors proposed an FPGA testbed for characterization analysis of error vector magnitude (EVM) for 5G communication. The OFDM symbol is pre-calculated and saved into random access memory (RAM) of the FPGA ZC706 of AMD-Xilinx, and post-processing offline using Matlab. Additionally, only 64-QAM modulation order with the bandwidth of 200 MHz and the fast Fourier transform (FFT) size of 1024 was considered. As can be seen, the testbed parameters are not 5G, which is detailed in [14]. In [15], the authors proposed phase noise equalization for OFDM at the carrier frequency of 60 GHz, in which the decision-directed method is employed. However, the transmitter OFDM processing is also precalculated in a C program and saved inside the FPGA. For the receiver processing, the work is also done by software in offline processing, and the FPGA is only for controlling the ADC to sample the received signal. The AMD-Xilinx Virtex-5 LX110T is used. Additionally, the only FFT size of 512 with 64-QAM is employed. From the literature review, the lack of real-time implementations can be the primary issue, and the FPGA implementation for phase noise is necessary. Recently, in [16], the data recovery from a clipped OFDM signal affected by phase noise is investigated. The authors developed a special function to optimize both the phase noise and the data. The variational message passing theory is the key aspect of the received information data, where the possibility of errors is considered. Both theoretical analysis and simulations confirm the effectiveness of this method. Additionally, in [17], the maximum a posteriori - autoregressive (MAP-AR) method for phase noise estimation in OFDM systems is proposed. The technique leverages the sparse structure of the AR process model, leading to efficient estimation via linear equations. Compared to existing techniques, MAP-AR demonstrates superior performance, making it a valuable tool for mitigating the effects of phase noise in OFDM. However, the complexity of the two proposed techniques is very high, and a lot of multiplications are required.

1.2. Main Contributions

To address the above challenges of real-time, high-throughput processing for phase noise compensation in 5G FR2 systems, the primary contribution of this work is the development of phase noise estimation utilizing MLE and equalization. This approach facilitates high-speed processing with a bandwidth of 400 MHz for the FR2 carrier in 5G OFDM through FPGA implementation. The choice of an FPGA-based architecture is fundamentally motivated by its intrinsic parallelism and reconfigurability, which are essential for fulfilling the rigorous real-time processing requirements of high-bandwidth signals. In contrast to application-specific integrated circuits (ASICs), FPGAs provide the flexibility to accommodate evolving standards and design modifications, while delivering markedly higher performance than software-based digital signal processing (DSP) board implementations for computationally demanding tasks. The real-time computations involved in phase noise estimation are demonstrated herein. Typically, an FPGA operates with an internal clock limited to a few 100 MHz; however, this constraint may vary depending on the complexity of the implementation. Consequently, implementing the direct method at such a large bandwidth is unfeasible. In response, this work proposes a parallel processing algorithm that reduces the clock speed to a few megahertz. Furthermore, the results have been validated through both MATLAB numerical simulations and testing based on FPGA experiments utilizing the Virtex-7 VC77 platform from AMD-Xilinx. The findings indicate a close agreement between simulation and experimental results, with minimal resource consumption even when executing eight parallel computations concurrently.

2. MLE method for phase noise estimation and equalization

Let the OFDM in time domain transmitted signal with a 400 MHz bandwidth of FR2 frequency carrier region. The received time domain OFDM signal, which is corrupted by fading channel and phase noise, is denoted by pn, is given by

$$y(n) = \left(x(n) * h(n)\right) e^{jpn(n)} + z(n), \tag{1}$$

where n is a discrete time sample, $h(n)$ is channel coefficient gain, $z(n)$ is the additive white Gaussian noise (AWGN) with the variant of s_z^2 and zero mean. $pn = f_{PN}(n)$ is a random phase noise component, modeled by Wiener process [18-19], with the variant of $s_v^2 = 2pvT_S$. v denotes the sum of the oscillator linewidth of the transmitter and receiver, and it is measured from the two-sided 3-dB linewidth of the Lorentzian power spectral density [18] and T_S is the sampling time. Each OFDM symbol has a CP that is long enough to neglect ISI.

To analyse the phase noise effect at the receiver end, for simplicity, $h(n)$ and $z(n)$ are first omitted or compensated for completely by channel estimation and the compensation process. Then, applying the FFT to Eq. (1), we get [21],

$$\begin{aligned} Y(k) &= FFT\left(y(n)\right) \\ &= X(k) \ddot{A} PN(k) \\ &= \sum_{k=0}^{N-1} X(k) \times PN(k-n) \\ &= \underbrace{X(k)PN(0)}_{for\ k=n} + \underbrace{\sum^{N-1} X(n)PN(k-n)}_{ICI} \end{aligned}, \tag{2}$$

where $X(k) = FFT(x(n))$, $k = 0...N-1$ and N is the size of the fast Fourier transform (FFT). The symbol $\ddot{A}$ is a linear convolution operator and $PN(k)$ are the received signal and the phase noise in the frequency domain, which is given by

$$PN(k) = \frac{1}{N} \sum_{n=0}^{N-1} pn(n) e^{j2pkn/N}, \tag{3}$$

hence, for $k = 0$, the $PN(0)$ is

$$\begin{aligned} PN(0) &= \sum_{n=0}^{N-1} pn(n) e^{j2p0n/N} \\ &= \frac{1}{N} \sum_{n=0}^{N-1} f_{PN}(n) \end{aligned}. \tag{4}$$

From (2), $PN(0)$ rotates the phase for all subcarriers. It is the so-called common phase rotation (CPR) or it can be considered as common phase error. Additionally, there are two terms. The first one is the deserted signal, which is destroyed by $PN(0)$. The second term is ICI, which is the noise effect on the whole subcarrier. As a result, the orthogonality for each subcarrier is lost.

The phase noise needs to be estimated and cancelled. Unfortunately, ICI remains, even $PN(0)$ is completely compensated. Assuming that the vector of CPR, denoted by Δ, is the set of $[PN_{p=0}(0)\ PN_{p=1}(0)...PN_{p=Np-1}(0)]$, in which its length is equal to the number of pilots on each OFDM symbol. Np is the number of pilots. Since the number of subcarriers is large enough, the Gaussian distribution of the Δ is given by

$$f(\Delta) = \frac{1}{\sqrt{2ps_{PN}^2}} e^{-\frac{1}{2}\left(\frac{\Delta - m_{PN}}{s_{PN}^2}\right)^2}, \tag{5}$$

where m_{PN} and s_{PN}^2 are the mean and variance of the estimated phase noise from Δ, respectively. Next, we need to sum up the log likelihood of Eq. (5) for each data element to evaluate our parameters throughout the entire Δ set, it is expressed by [22]

DOI:10.4186/ej.2025.29.8.67

$$\sum_{p=0}^{Np-1}\log\left(f(\Delta)\right)=\sum_{p=0}^{Np-1}\log\left(\frac{1}{\sqrt{2\pi\sigma_{PN}^2}}e^{-\frac{1}{2}\left(\frac{PN_p(0)-\mu_{PN}}{\sigma_{PN}^2}\right)}\right)$$

$$=-\frac{N}{2}\log(2\pi\sigma_{PN}^2)-\frac{1}{2\sigma_{PN}^2}\sum_{p=0}^{N-1}\left(PN_p(0)-\mu_{PN}\right). \quad (6)$$

Then, the maximum of the log likelihood is achieved by differentiating Eq. (6) with respect to m_{PN} and then set it to zero, $\frac{\P}{\P m_{PN}}\sum_{p=0}^{Np-1}\log(f(\mathrm{D}))=0$. Then, we get maximum of the log likelihood, which is $m_{PN}=\frac{1}{Np}\sum_{p=0}^{Np-1}PN(0)$. By comparing with the CPR, in this case, the estimated CPR is

$$\hat{y}=\frac{1}{Np}\sum_{p=0}^{Np-1}\bar{P}N_p(0), \quad (7)$$

where $\hat{y}$ is the estimated CPR, and from Eq. (2) and Eq. (7). $\bar{P}N_p(0)$ can be calculated by

$$\bar{P}N_p(0)=\frac{Yp(m)}{Xp(m)}=\frac{Xp(m)PN_m(0)}{Xp(m)}+\frac{1}{Xp(m)}\sum_{n=0,n\neq m}^{N-1}X(n)PN(m-n)$$
$$=PN_p(0)+z \quad (8)$$

Hence, $Yp(m)$ and $Xp(m)$ are the received and known transmitted pilot data for the mth pilot subcarrier location, respectively. $z=\frac{1}{Xp(m)}\sum_{m=0,m\neq n}^{N-1}X(n)PN(m-n)$, which is a complex Gaussian distribution with zero mean and a variance is s_z^2 [22-23]. The final process is equalization, accomplished by conjugating Eq. (7) and multiplying it back to the received signal, as well as dividing by its own power. This implies that,

$$\hat{Y}(k)=Y(k)\times\frac{\hat{y}^*}{|\hat{y}|^2}, \quad (9)$$

where $(\,)^*$ is conjugation operator. $\hat{Y}(k)$ is the estimated received symbol is.

3. 5G pilot Location

Pilot location of 5G FR2 is discussed in this section. 5G with carrier region of FR2 with subcarrier spacing of 120 kHz and 66 pilot data are employed [23]. The pilot is so-called PT-RS (Phase tracking reference signals); thus, from Eq.(7), $Np=66$ and $m=0...65$. The PT-RS location and alignment are shown in Fig. 1, where the DMRS is the demodulation reference signal and DL-CCH is the downlink control channel. For the uplink, the pilot starts at the subcarrier bin of $13+48(0)$ $13+48(1)$

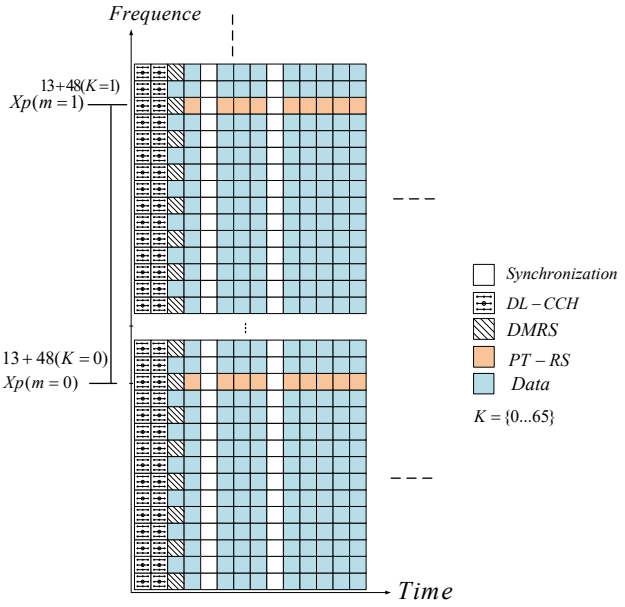

Fig. 1. Example of 5G frame structure for data and pilot location mapping.

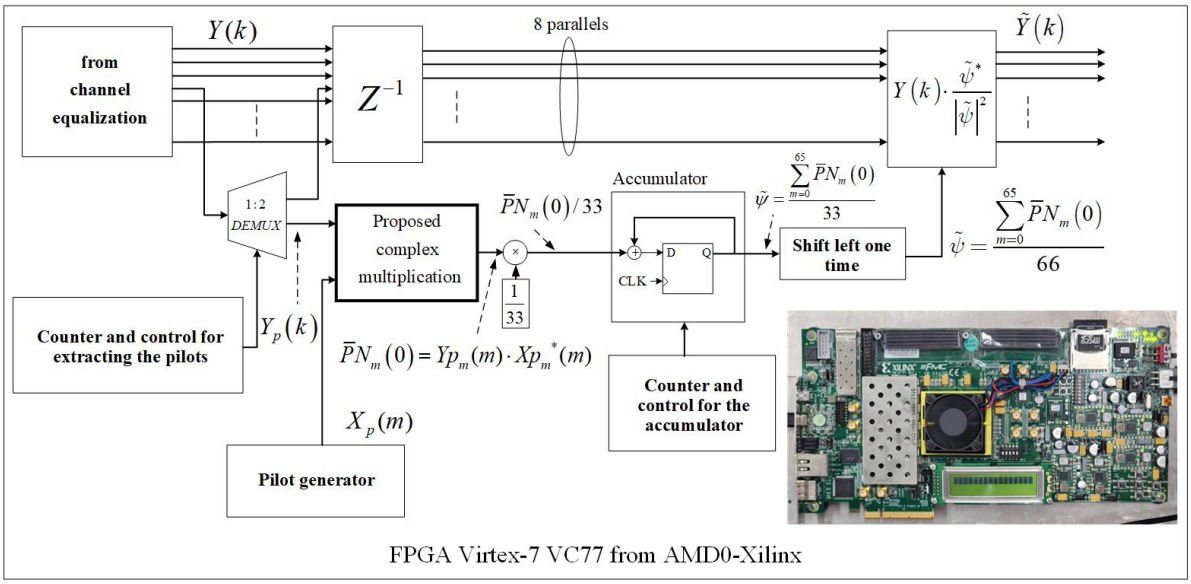

Fig. 2. Proposed FPGA implementation of ML phase noise estimation and compensation.

$13+48(2)$ … $13+48(K)$, where $K=1,...,66$. Additionally, quadrature phase-shift keying (QPSK) is used as PT-RS, where the detail of pilot mapping is provided in [1,23].

4. FPGA Implementation for MLE Method

In this section, an FPGA implementation using parallel processing is presented, as shown in Fig. 2. There are two main details that need to be discussed. First, the aspects of MLE in 5G OFDM mapping is shown. Second is the details of FPGA implementation is detailed.

4.1. MLE in 5G OFDM Implementation Method

From Eq.(7) – Eq.(9), in this case, $Np=66$; thus, the estimated CPR can be calculated by $\hat{y}=\frac{1}{66}\sum_{p=0}^{65}\bar{P}N_p(0)$

To get $\bar{P}N_p(0)$, from Eq.(8), the received pilot is divided by $Xp(m)$. However, since the power of the pilot is unity, its inversion equals to its own conjugation, $1/Xp(m)=Xp^*(m)$. As a result, only the multiplication between the conjugated data pilot and the received pilot is required. Then, the estimated phase $\bar{P}N_p(0)$ on each pilot location pth can be acquired.

4.2 FPGA Implementation

For FPGA implementation, high-speed processing is considered. The 8 parallel processing processors is proposed. Since the target bandwidth is 400 MHz in FR2 band, the internal clock usage in this work is only 50 MHz. Additionally, the fixed-point number is employed, where the word length of 18 bits with the fractional is 13 bits is used. The implementation is based on the FPGA evaluation board VC77 from AMD-Xilinx equipped with Virtex-7 technology, as shown in the insect of Fig. 2. The data stream from the channel estimation and compensation output is split into two branches. One is fed to the delay line to wait for the phase noise estimation calculation. The second branch is fed to the phase noise estimation process according to Eq. (7) - Eq. (9).

The received pilots are corrected based on their respective insertion locations through the utilization of a multiplexer. To get $\bar{P}N_m(0)$, the pilot $Yp(m)$ is multiplied with $Xp^*(m)$, as a results $\bar{P}N_m(0)=Yp(m)\cdot Xp_m^*(m)$. From the 5G release 17 [24], the pilot is generated by m-sequence code and mapped into QPSK, where the arbitrary symbol is $1/\sqrt{2}\times\{1+1i,1-1i,-1+1i,-1-1i\}$. In this work the pilot is pre-calculated in Matlab and stored into the internal ROM.

The $\bar{P}N_m(0)$ is next multiplied with a constant $1/33$, where it is precalculated by Matlab and saved to ROM. In another way round, the $\bar{P}N_m(0)$ can be divided by 66 directly; however, it would be lower accuracy since the $\bar{P}N_m(0)$ is too much attenuation. As a result, noise would

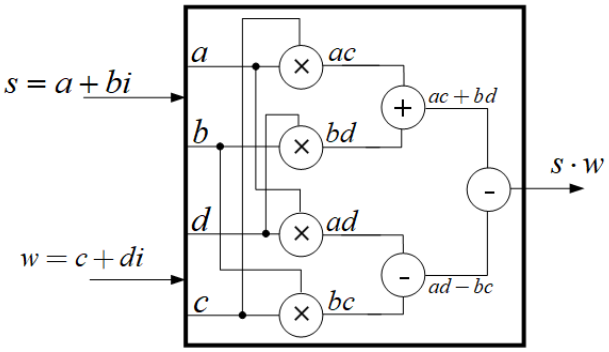

Fig. 3. Proposed complex multiplication with conjugation.

be dominated to the estimated phase. After dividing, the output accumulated for 66 time. The collected phase is divided by 2 again, where only shift left one time is needed and no logic gate consumption is required. Additionally, the accumulation will be reset before the next OFDM symbol comes. Then, the CPR , $\hat{y}$, can be calculated.

In the final step, by taking the $\hat{y}$ and multiplied it back to the delayed received signal for all subcarriers. Additionally, $|\hat{y}|^2=1$ since the scale power is done by channel estimation. Therefore, from Eq. (9), the CPR can be cancelled by using only $\hat{Y}(k)=Y(k)\times\hat{y}$, and it is done in 8 parallel simultaneously. Thus, the speed of 400 Msps in total can be achieved. Additionally, the calculation of $\hat{Y}(k)$ needs two processes, which are included of two's complement for conjugation operator and complex multiplication. However, to reduce logic gates, in this work, only complex multiplication is proposed, as presented in the next section.

4.3 Proposed Complex Multiplication with Conjugation Mathematics

The proposed complex multiplication of two complex number with conjugation is shown in Fig. 3. For the sake of simplicity, two notation $s=a+bi$ and $w=c+di$ are introduced. Thus, the complex multiplication is $s\times w=(ac+db)+(ad+bc)i$. As can be seen, by only changing the sign of the second term, the conjugation process can be omitted, and the expression is obtained by,

$$s\times w^*=(ac+db)+(ad-bc)i=(ac+db)-(ad-bc)i \quad (10)$$

DOI:10.4186/ej.2025.29.8.67

From Eq. (10), the two's complement operator is omitted, and only four real multiplications is needed for $Y(k)$ computation.

5. System Performance Results

This section presents the system performance, wherein numerical simulations conducted using Matlab are compared with experimental in FPGA results. Following RF demodulation, the baseband signals of the in-phase (I) and quadrature (Q) components are sampled at a rate of 400 MHz using an analog-to-digital converter (ADC). The remaining parameters, adhering to 5G Release 17 specifications for the maximum bandwidth scenario, are detailed in Table I. The received OFDM symbols, exclusively considering phase nose effects and additive white Gaussian noise (AWGN), are precomputed via Matlab and stored in the internal ROM of the FPGA. An AMD-Xilinx Virtex-7 FPGA evaluation kit VC707 is utilized for this purpose.

The BER performance with respect to SNR is investigated as well as performance comparison to FPGA implementation is presented. The results are depicted in Fig. 4. Two points of investigation are presented. First, the performance of phase noise estimation using proposed MLE is evaluated and compared with the common phase rotation method from equation (16) in [25]. Considering the 16-QAM, as can be seen, the BER from the proposed MLE and from [25] are somewhat similar for both linewidth variant of $s_v = 1.3' 10^{-3}$ and $s_v = 2.8' 10^{-3}$. However, the proposed MLE method is much simpler since only constant of $1/66$ is needed for the denominator, while the common phase error method needs summed pilot signal power computation. Additionally, for $s_v = 1.3' 10^{-3}$, the BER is very close to the theoretical optimal curve, which is calculated from [26]. The SNR difference is less than 2 dB at the BER of 10^{-5}. The second aspect considers the comparison of bit error rate (BER) between simulation and implementation. Please refer to Fig. 4 for the 64-QAM and 256-QAM orders, the blue line with square and star markers represents the simulated BER performance, while the red dashed line with star and circle markers represents phase noise equalization using FPGA implementation. Please note that the experimental BER cannot be done for all SNR since the experimental information is very huge. The input OFDM symbols to the proposed algorithm for the SNR of 20 dB, 24 dB, 30 dB, and 34 dB are obtained as an example to compare with the simulated methods. The results show that the BER is reduced as the SNR increases for all QAM orders. Especially, the BER performance of simulation and FPGA implementation are minor different. Considering at the SNR=34 dB with 64-QAM, the BER of 2.5×10^{-4} for simulation, while 4.5×10^{-4} for implementation are achieved, respectively. As can be seen, the FPGA implementation is well matched with the simulation one.

Table I. Simulation parameter for 5G OFDM phase noise analysis

Parameter	Value
Carrier frequency	28GHz
Phase noise variant (s_v)	$1.3' 10^{-3}$
FFT size (N)	4096
CP length	288
Subcarrier spacing	120 kHz
Bandwidth	400MHz
Modulation	16-, 64- and 256-QAM
Effective subcarrier	3,300
Noise	AWGN

Next, to enhance its realism, the Rician and Rayleigh channel of 8 tabs with 64-QAM are included. The Rician K-factor of -20 dB, 0 dB and 5 dB are investigated. The phase noise variant of $s_v = 1.3' 10^{-3}$ is assumed. The least mean square with cubic spline interpolation is used for channel estimation and compensation. The detail is in [27], and that is out of the scope of this work. The result is depicted in Fig. 5. As can be seen, when the Rician K-factor is reduced, the BER is reduced. Additionally, at the K-factor of -20 dB, the BER of Rician and Rayleigh channel are slightly the same. However, the BER of the Rician channel considered to more than the BER of Rayleigh channel. Reconnect to Fig. 4, the BER performance is increased. However, the BER below 10^{-3} can be achieved. This suggests that if we apply

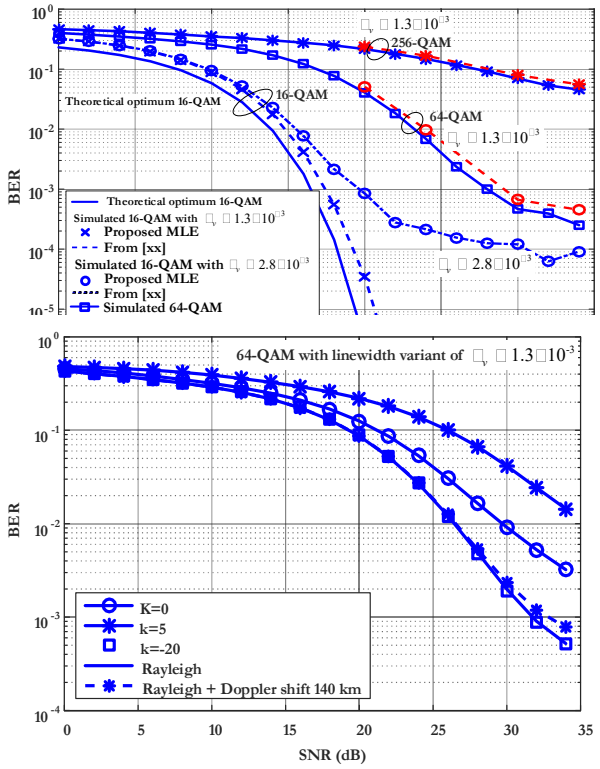

Fig. 5. BER performance against SNR with Rician and Rayleigh channel of 8 tabs with a Doppler shift of 140 km is considered.

feedforward error correcting [28] code, the BER free is possible. Furthermore, the Doppler shift effect in a Rayleigh environment is included in the analysis, where the speed of 140 km/h is considered. As can be shown, the BER is slightly higher than in the case of only Rayleigh fading. The BER confirms that the proposed method performs well under strong wireless channel conditions. Additionally, from Figs. 4 and 5, the BER performance effectively corresponds to 5G use cases of ultra-reliable low latency communications (URLLC), where requirements for ultra-high reliability, BER $<10^{-5}$, are met at higher SNRs, while AR/VR enhanced mobile broadband (eMBB) applications are supported by higher QAM orders, achieving typical data-centric BERs from 10^{-3} to 10^{-4}. For massive machine-type communications (mMTC), our results demonstrate acceptable BERs even at lower SNRs, confirming its suitability for massive, energy-efficient deployments. Notably, the system does not yet include error-correcting codes; therefore, after error correction, the BER should be lower than the current value.

Figure 6 displays 64-QAM constellations illustrating PN effects and the performance of the proposed equalization. Fig. 6A shows the received signal severely distorted in both amplitude and phase by uncompensated PN at 35 dB, characterized by a distinct circular smearing of symbols. Fig. 6B demonstrates the significant restoration of the constellation points after applying the proposed PN equalization at the same 35 dB SNR. Finally, Fig. 6C presents the constellation after PN equalization at a higher 40 dB SNR, visibly showing even tighter symbol clustering. This progression clearly validates the effectiveness of the equalization method in reducing phase noise and improving signal quality across different noise conditions.

Figure 7 presents a ChipScope Pro recording of the FPGA implementation performing phase noise compensation in running real-time. 64-QAM modulation with SNR of 34 dB is employed. The In-phase (I) and Quadrature (Q) components of the OFDM signal are showed in signed decimal format (see A) and the BER

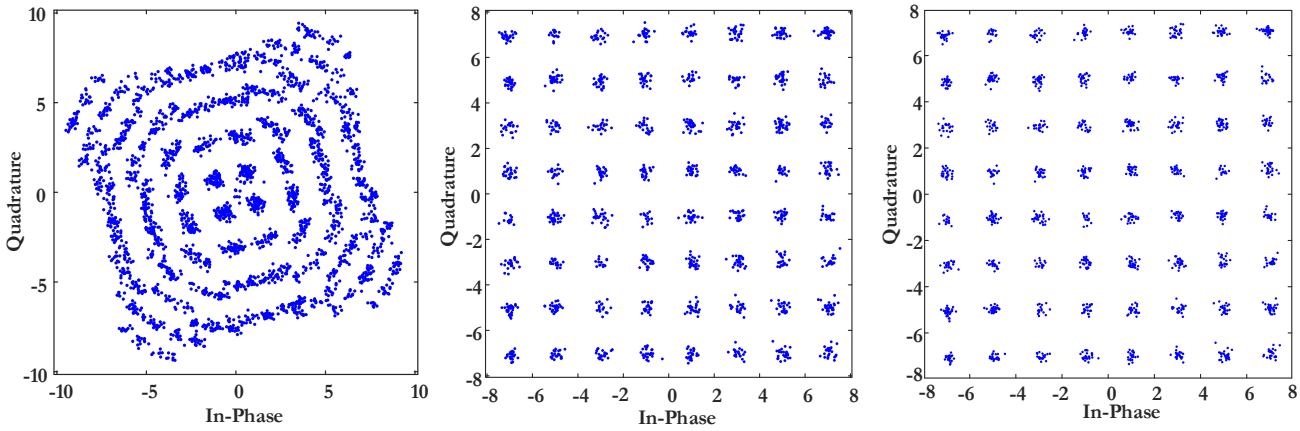

Fig. 6. Received signal after Droppler effect of 90 km/h and Rician channel for 64-QAM constellation where:
A. Constellation with uncompensated PN at 35 dB SNR.
B. Constellation after proposed PN equalization at 35 dB SNR.
C. Constellation after proposed PN compensation at 40 dB SNR.

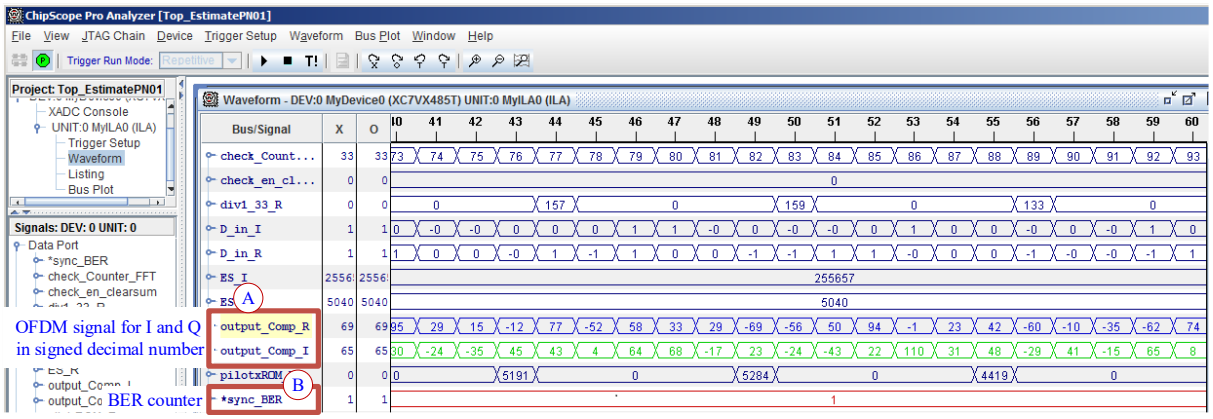

Fig. 7. ChipScope Pro snapshot of the FPGA running for the real-time phase noise compensation:
A. OFDM signal for both real and imaginary.
B. BER counter

DOI:10.4186/ej.2025.29.8.67

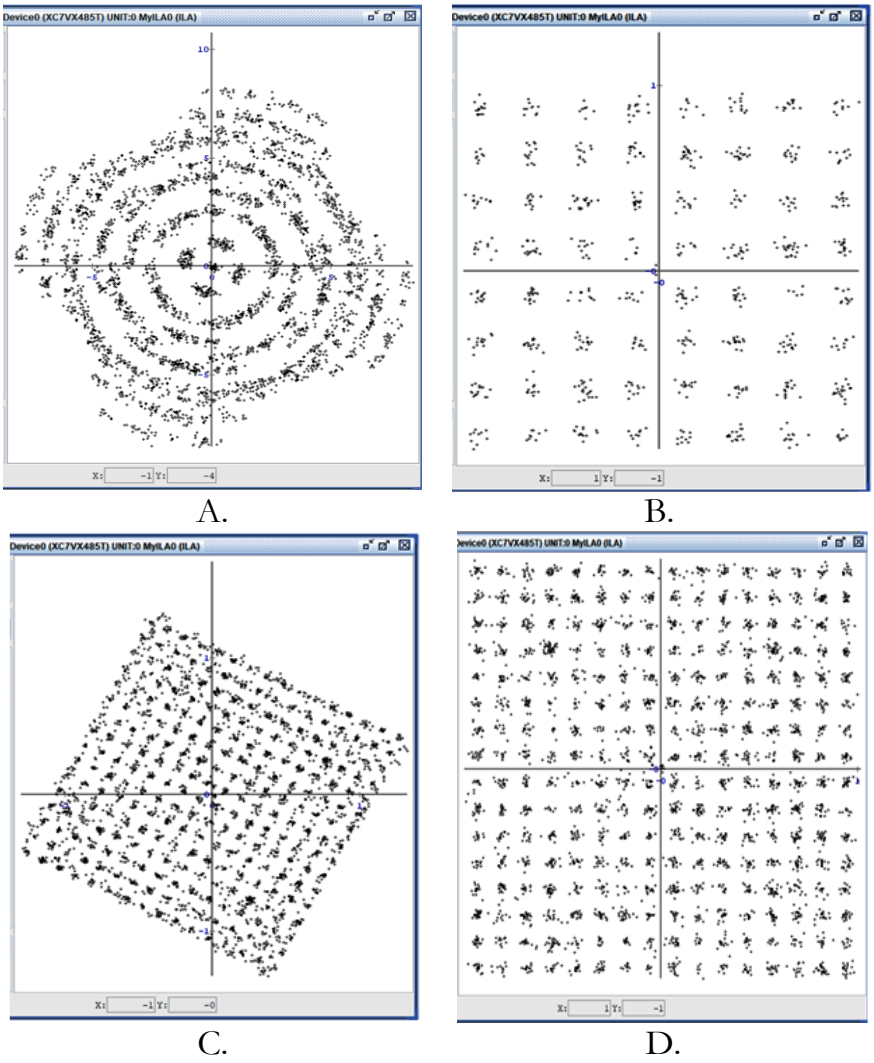

Fig. 8. Captured the constellation from by Chip-scope Pro at SNR of 34 dB and $s_v = 0.0013$:
A. Without compensating for 64-QAM
B. With compensating for 64-QAM
C. Without compensating for 256-QAM
D. Wit compensating for 256-QAM

count (see B). These results indicate that the real-time operation of the system is successfully achieved.

Figure 8 further verifies the real-time implementation on the FPGA. ChipScope Pro captures the calculations performed by the FPGA in real-time, without any offline processing. 64-QAM and 256-QAM input at the SNR=34 dB is employed. The left-hand Fig. 8A and Fig. 8C show the uncompensated phase noise, while the right-hand Fig. 8B and Fig. 8D demonstrate the equalized signals. As evident, the phase rotation is corrected and returned to the correct position. Please note that the maximum buffer depth of ChipScope Pro is limited to 4096 samples.

This limitation affects the visualization of the 256-QAM signal, which exhibits a more random-looking phase rotation compared to the clearer rotation seen in the 64-QAM case. Nevertheless, the successful FPGA implementation and excellent system performance are evident.

Finally, Table II summarizes the resource consumption of the FPGA implementation. The occupied slices represent only 3% of the available resources, while the number of slice registers consumes barely 1%. This low resource utilization indicates variable space for accommodating additional OFDM processing tasks on the same FPGA. This minimal resource consumption is a major advantage because it leaves ample capacity for adding extra functionalities in the future, such as further impairment compensation, MIMO processing, or multi-channel support, on the same FPGA. This is confirmed that the proposed solution highly appealing for complex integrated 5G FR2 baseband processing systems. Moreover, the study effectively demonstrates the success of the proposed phase noise compensation algorithm. From all results, both on simulations and FPGA implementation validate its ability to mitigate phase noise in an OFDM system. Although the algorithm effectively compensates for the CPR, ICI cancellation remains a

Table II. FPGA Virtex-7 resource usage

Parameter	Value
Number of occupied Slices	3%
Number of Slice Registers	1%
Number used as Memory	3%
Number of DSP48E1s	1%

challenge. This residual ICI contributes to the BER observed in the system. The more bit resolution would be needed when the higher order QAM is employed as studied in [29]. Additionally, the decision-feedback phase noise equalizer [30] provides also well compensation performance. However, the algorithm involves the integration of decision-making circuits, feedback loops, and equalization filters, which is impossible to implementation for high speed communication systems.

6. Conclusion

The phase noise cancellation for high-speed 5G OFDM using the MLE method was successfully implemented on an FPGA. To overcome FPGA clock speed limitations for 400 MHz bandwidth, a parallel processing algorithm was proposed, enabling operation with significantly lower internal clocks. An optimized complex multiplication also reduced logic gate usage. Numerical simulations and real-time FPGA running on a Virtex-7 VC77 board both confirmed excellent performance, achieving BER below 10^{-3} for 16-QAM and 64-QAM. The FPGA implementation results strongly correlated with simulations, demonstrating the robustness and practical viability of our design. Furthermore, the high efficiency is evident, consuming only 3% of FPGA slices. This work primarily focused on phase noise, and a significant reduction in phase noise was achieved. Future work will extend this framework to address other impairments like residual ICI, explore its application in complex systems such as multiple-input multiple-output (MIMO), and investigate further power consumption optimizations. This efficient FPGA implementation is a crucial step toward robust and energy-efficient 5G FR2 communication systems.

Acknowledgement

This research project is supported by Science Research and Innovation Fund. Contract No. FF66-P1-055.

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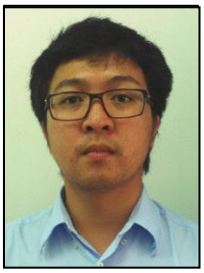

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