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Article

Design and Performance Analysis of New Seventeen Level Reduced Switch Count Multilevel Inverter

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Abstract. Multilevel inverter has emerged newly as a very important alternate in the area of high-power medium-voltage energy control. The main problem in this technology is high devices, total standing voltage, cost, THD and efficiency. This paper's main goal is to provide a 17-level multilevel inverter with only 8 switches and 4 diodes. Four different unequal DC sources are used in this arrangement to produce the output voltage waveform with 17 levels. For the proposed inverter, the cost function per level, efficiency, total standing voltage, conduction losses, and switching losses have all been calculated in detail. Typical inverters have higher switching losses, prices, and harmonic distortion because they have more semiconductor power switches, diodes, capacitors, driver circuits, and DC sources. The switching components of the suggested arrangement have been controlled using the nearest-level control approach. The suggested multilevel inverter offers a higher efficiency of 98.24%, cost function of 5.7 for a weight coefficient of 1, improved power quality, and higher reliability. The total harmonic distortion produced by this inverter is 3.43%, which comes under the IEEE standard of 5%.

Keywords: Multilevel inverter, nearest level control, total harmonic distortion, pulse width modulation, cost function, total standing voltage.

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1. Introduction

Multilevel inverters are commonly used in FACTS devices, Battery-powered EVs, and Smart grids due to features such as decreased dv/dt stress, adaptability, and improved power quality. They are highly suited for these applications due to their ability in producing high terminal output voltages utilizing low and medium voltage components [1, 2]. Multilevel inverters are generally classified as one of the three types: Diode Clamped or Neutral Point Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI). DCMLI demands greater number of diodes as the levels in output waveform increases, as well as a large number of power components, making circuit management complex. The voltage balance issue created by diodes in DCMLI can be addressed in FCMLI by utilizing redundancy in switching states provided by clamping capacitors; however, higher number of passive circuit components would decrease circuit reliability [3-6]. If compared to other two topologies, CHBMLI is extremely modular and easier to regulate. Furthermore, it uses separate DC sources, hence need for voltage balancing circuits is eliminated. Nonetheless, every additional DC source raises the need for number of power electronic power switches by four in standard CHB-MLI. The requirement of more power devices in traditional topologies has pushed the door for research into increased level of inverter called multilevel inverter configurations with fewer power devices [7-9].

The concept of using switched DC input voltages to add level and polarity reversal through H-Bridge is at the heart of most setups that use autonomous DC sources for synthesizing levels in output waveforms. As the entire blocking output across the H-Bride is four times the DC input voltage, the number of components rises. [10].

This paper discusses an unique multilayer inverter arrangement. n+5 power switches are required for 'n' independent sources. Because of the increased levels in terminal voltage waveform, the blocking voltage across power switches in polarity changer rises considerably. It is necessary to use power switches with the greatest voltage requirements and bigger heat sink [8-9].

An architecture that uses four-quadrant power switch design that allows switching circuitry to function in both balanced and unbalanced modes. The arrangement has high number of power switches, resulting in greater losses [14]. Due of their distinct characteristics, multilevel inverters are gaining traction in a wide range of low- to high-voltage, high-power applications. Multilevel inverters offer several benefits, including reduced voltage stress and semiconductor device loss, improved power quality, and reduced electro-magnetic interference. The main challenges with multilevel inverters are voltage balance, a rise in the number of semiconductor switches and capacitors, and more precise control [11-13]. Despite the fact that MLIs have been used in traction drives in number of studies, they have yet to be widely used in low-power electric transportation. These configurations are used in high-power electric ships and trains, as well as low-power vehicles such as passenger EVs and electric buses. They employ typical two-level inverter due to reduced DC-link voltage, ease of design, and implementation. [14-16]. Seven-level switched capacitors with a single input source inverter have been proposed. TSV and CF per level are high when they are increased to more levels [17]. 11 switches, a single source, two capacitors, and a 15-level inverter have been proposed. The efficiency is 95.3%, THD is 3.18%, and TSV is 4.62 [18]. A novel five-level switched capacitor MLI is proposed, which provides more THD, TSV, and CF per level [19]. 16 switches, 2 DC sources, and 2 capacitors with 17-level MLI are implemented. The efficiency of the proposed MLI is 95.54%, and THD is 6.4 % [20]. A new switched capacitor-based six switches 5 level MLI is proposed. It uses only one power source and two SCs to obtain a five-level output voltage. THD is more than 5%, and TSV and CF per level are high [21]. 11 levels with 11 switches and 4 sources of MLI are presented; the THD of the proposed MLI is 7.14, and the efficiency of the MLI is 96.29 % [22]. 12 switches, 5 DC sources 22 level MLI is presented. The efficiency of the MLI is 97.31 %, and THD is 5.02 % [23]. 21 level MLI is proposed with 20 switches and 6 DC sources. THD of the MLI is 3.9%. TSV and CF per unit are high [24]. 11 switches, 4 DC sources 31-level MLI is proposed, THD is 3.34 %, and efficiency is 93.51 % [25].

The New MLI that combines concepts of multi-conversion cell and H-bridge which makes both positive and negative polarity. The suggested configuration's key design features are,

- Has smaller number of components - 8 switches.
- More levels - 17 levels.
- Less total harmonic distortions.
- Switching Losses and conduction losses are less.
- Efficiency is more.
- Total Standing voltage and Cost function is less.
- Complexity of the circuits is less.

2. Conventional Multilevel Inverters

To produce multilevel output voltage neutral point clamped (NPC) or DCMLI has been shown in Fig. 1a. In this configuration power switches are connected in series and the diodes as clamping elements to create a desired levels in the output. NPC-MLI is flexible to control and since it utilizes diodes for clamping, costs are lower. To achieve a waveform with m levels in the output voltage, DC-link capacitors are needed.

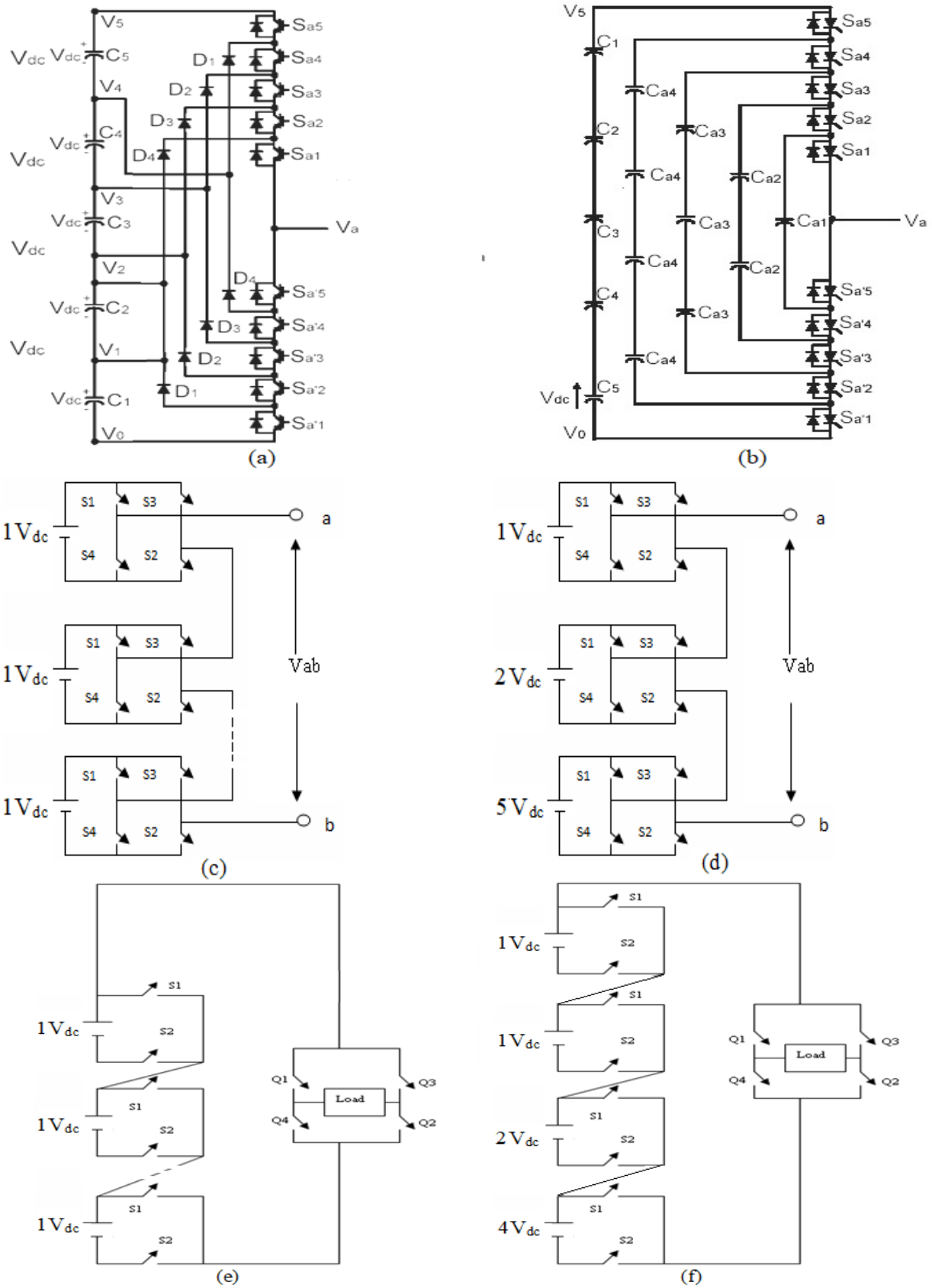

Fig. 1. a) Diode Clamped MLI, b) Flying Capacitor MLI, c) Cascaded H bridge MLI, d) Hybrid MLI, e) New Cascaded MLI, f) New Hybrid MLI. [26-30]

Each phase needs 2(m−1) power switches and (m−1) (m−2) diodes. There is an unbalanced stress on switches throughout the operation of NPC-MLI. It requires a more diodes and power switches. Moreover, this NPC-MLI needs one central and one high DC-link voltage while raising the inverter power. The next topology is flying capacitor multilevel inverter (FCMLI) as shown in figure 1b, In this topology flying capacitors are used as a replacement for of clamped diodes and it is safe and more easy to control and delivers pure output waveform. The FCMLI is also easy to control because it utilizes capacitors as clamping elements. The power dissipation in this MLI is equally divided among all switches. The FCMLI needs higher switching frequencies and balanced clamping capacitor voltages at high DC-link voltage. Complexity and costs of this inverter are higher when compared to NPC-MLI since the capacitors are more expensive than diodes. Alternatively, cascaded H-bridge multilevel inverter (CHBMLI) topology is that which involves multiple symmetrical DC sources with H-bridges as shown in Fig. 1c. The same circuit with unsymmetrical sources is stated as hybrid multilevel inverter shown in figure 1d. Each H-bridge involves four number of switches. Figure 1e & 1f shows the new cascaded MLI which involves two stages; first stage is two power switches with symmetrical or unsymmetrical voltage sources which can be extended easily to produce more levels. Second stage is polarity conversion cell that is H bridge which converts stepped DC waveform into AC waveform.

3. New Reduced Switch Count Multilevel Inverter (NRSCMLI)

Figure 2 depicts the structure of proposed topology which consist of four power switches and four diodes with four unsymmetrical voltage sources $1V_{dc}$, $1V_{dc}$, $2V_{dc}$ and $4V_{dc}$. This produces unidirectional stepped 17 level output voltage or current waveform which is further connected with the H bridge circuit to produce alternative output. Unsymmetrical DC sources are obtained from DC sources by using DC-DC conversion techniques. The key benefit of the suggested MLI is that it has seventeen number of levels while using only eight power switches. The operation of proposed multilevel is:

Mode 1: Switches S_5 & S_7, or S_6 & S_8 conduct and it produces zero output voltage.
Mode 2: Switches S_1, and diodes D_2, D_3, D_4 conduct and produces $1V_{dc}$=28V, it supplies to the load.
Mode 3: Switches S_3, and diodes D_1, D_2, and D_4 conduct and produces $2V_{dc}$=56V, it supplies to the load.
Mode 4: Switches S_2, S_3, and diodes D_1 & D_4 conduct and produces $1V_{dc}+2V_{dc} = 3V_{dc}$ =84V to the load.
Mode 5: In this mode switch S_4 is turned ON and switches S_1, S_2, S_3 are turned OFF and diodes D_1, D_2, and D3 conduct produces $4V_{dc}$=112V across the load.
Mode 6: Switch S_1, S_4 and diodes D_2 and D_3 conducts and produces $5V_{dc}$=140V, it supplies to the load.
Mode 7: Switches S_3, S_4 and diode D_1 and D_2 conduct and the output voltage across the load is $6V_{dc}$=168V.
Mode 8: Switches S_2, S_3, S_4 and diode D_1 conduct and the output voltage across the load is $7V_{dc}$=196V.
Mode 9: Switches S_1, S_2, S_3 and S_4 conduct and now the output voltage is $8V_{dc}$=224V.

The mode 1 to 9 will repeat and during positive half cycle switches S_5 and S_7 conduct and during positive half cycle switches S_6 and S_8 conduct. Table 1 illustrate the operation of NRSCMLI for all modes including positive and negative half cycles.

3.1. Estimation of Loss and Efficiency

This section describes the theoretical calculation of loss used to determine efficiency of recommended inverter. The most significant losses are conduction and switching losses, and its calculation is based on the assumption that load is totally resistive and that voltage available at the inverter output terminal is staircase output waveform. Conduction loss happens when MOSFET power switches are actuated and conducts electricity in a multilevel inverter. In the proposed inverter design, each MOSFET power switch used in the polarity transformation unit is computed individually to determine total loss during conduction. In the suggested inverter, power switches are used as a polarity conversion unit, and load current in a single phase is measured with regard to neutral. In this case, loss due to switch conduction period during the basic cycle quarter is calculated.

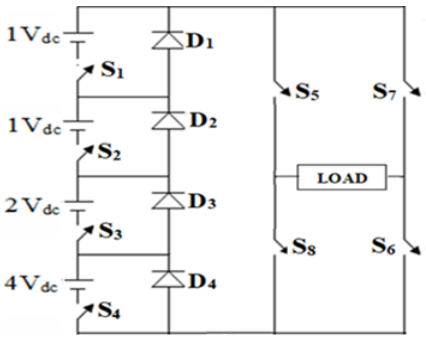

Fig. 2. New Reduced Switched Count multilevel inverter.

$$P_{CON} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} {I_R}^2(t)\, R_{ON,}Tdt \quad (1)$$

The transistor's on-state resistance and load current are denoted as $R_{on}T$ and $I_R(t)$, respectively. By employing a high number of auxiliary units, the proposed system provides 17 levels of output voltage, and the current in the load side is sinusoidal. As a result, the load current is expressed as

$$I_R = I_{P,}sinwt \quad (2)$$

Using (1) and (2), the average loss of single-phase system during conduction is derived as,

$$P_{CON1} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} I_{P,}{}^2 sin^2\, wtR_{ON,}Tdt \quad (3)$$

Throughout the basic cycle, MOSFET switches in the multi-conversion unit are turned on. For the cycle period of π, the loss in multi-conversion is as

$$P_{CON2} = \frac{1}{\pi}\int_0^{\pi} I_{P,}{}^2 sin^2\, wtR_{ON,}Tdt \quad (4)$$

The proposed multilevel inverter has one multi-conversion unit, and the loss during conduction is calculated as follows.

$$P_{CON,TOTAL} = P_{CON1} + P_{CON2} \quad (5)$$

During the transition from ON to OFF or vice versa, the overlapping of voltage and current produces switching loss in MOSFET power switches. The energy loss of MOSFET power switches is computed as follows throughout their on and off periods:

$$E_{ON} = \frac{V_{ON}\times I}{6}\, T_{ON} \quad (6)$$

where V_{ON}, I, T_{ON} are the MOSFET on-state voltage, the MOSFET current after switching on and turn on time respectively.

$$E_{OFF} = \frac{V_{OFF}\times I}{6}\, T_{OFF} \quad (7)$$

Table 1. Switching Configuration of NRSCMLI.

Modes		Load Current Path												Output	
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	D_1	D_2	D_3	D_4	Voltage(V)	
Positive Half Cycle	1	0	0	0	0	1	0	1	0	OFF	OFF	OFF	OFF	$0V_{dc}$	0V
	2	1	0	0	0	1	1	0	0	OFF	ON	ON	ON	$1V_{dc}$	+28V
	3	0	0	1	0	1	1	0	0	ON	ON	OFF	ON	$2V_{dc}$	+56V
	4	0	1	1	0	1	1	0	0	ON	OFF	OFF	ON	$3V_{dc}$	+84V
	5	0	0	0	1	1	1	0	0	OFF	OFF	OFF	ON	$4V_{dc}$	+112V
	6	0	1	0	1	1	1	0	0	ON	OFF	ON	OFF	$5V_{dc}$	+140V
	7	0	0	1	1	1	1	0	0	OFF	OFF	ON	ON	$6V_{dc}$	+168V
	8	0	1	1	1	1	1	0	0	ON	OFF	OFF	OFF	$7V_{dc}$	+196V
	9	1	1	1	1	1	1	0	0	OFF	OFF	OFF	OFF	$8V_{dc}$	+224V
	10	0	1	1	1	1	1	0	0	ON	OFF	OFF	OFF	$7V_{dc}$	+196V
	11	0	0	1	1	1	1	0	0	ON	ON	OFF	OFF	$6V_{dc}$	+168V
	12	0	1	0	1	1	1	0	0	ON	OFF	ON	OFF	$5V_{dc}$	+140V
	13	0	0	0	1	1	1	0	0	ON	ON	ON	OFF	$4V_{dc}$	+112V
	14	0	1	1	0	1	1	0	0	OFF	ON	ON	OFF	$3V_{dc}$	+84V
	15	0	0	1	0	1	1	0	0	ON	ON	OFF	ON	$2V_{dc}$	+56V
	17	1	0	0	0	1	1	0	0	OFF	ON	ON	ON	$1V_{dc}$	+28V
	18	0	0	0	0	1	1	1	0	OFF	OFF	OFF	OFF	$0V_{dc}$	0V
Negative Half Cycle	19	0	0	0	0	0	1	0	1	OFF	OFF	OFF	OFF	$0V_{dc}$	0V
	20	1	0	0	0	0	0	1	1	OFF	ON	ON	ON	$-1V_{dc}$	-28V
	21	0	0	1	0	0	0	1	1	ON	ON	OFF	ON	$-2V_{dc}$	-56V
	22	0	1	1	0	0	0	1	1	ON	OFF	OFF	ON	$-3V_{dc}$	-84V
	23	0	0	0	1	0	0	1	1	OFF	OFF	OFF	ON	$-4V_{dc}$	-112V
	24	0	1	0	1	0	0	1	1	ON	OFF	ON	OFF	$-5V_{dc}$	-140V
	25	0	0	1	1	0	0	1	1	OFF	OFF	ON	ON	$-6V_{dc}$	-168V
	26	0	1	1	1	0	0	1	1	ON	OFF	OFF	OFF	$-7V_{dc}$	-196V
	27	1	1	1	1	0	0	1	1	OFF	OFF	OFF	OFF	$-8V_{dc}$	-224V
	28	0	1	1	1	0	0	1	1	ON	OFF	OFF	OFF	$-7V_{dc}$	-196V
	29	0	0	1	1	0	0	1	1	ON	ON	OFF	OFF	$-6V_{dc}$	-168V
	30	0	1	0	1	0	0	1	1	ON	OFF	ON	OFF	$-5V_{dc}$	-140V
	31	0	0	0	1	0	0	1	1	ON	ON	ON	OFF	$-4V_{dc}$	-112V
	32	0	1	1	0	0	0	1	1	OFF	ON	ON	OFF	$-3V_{dc}$	-84V
	33	0	0	1	0	0	0	1	1	ON	ON	OFF	ON	$-2V_{dc}$	-56V
	34	1	0	0	0	0	0	1	1	OFF	ON	ON	ON	$-1V_{dc}$	-28V
	35	0	0	0	0	0	0	1	1	OFF	OFF	OFF	OFF	$0V_{dc}$	0V

V_{OFF}, I_{OFF}, and T_{OFF} are the MOSFET off-state voltage, current passing through the MOSFET before it turns off, and turn-off time, respectively. The switching power loss in the proposed MLI is calculated individually for each power switch in each unit using equations (6) and (7). The polarity conversion unit's MOSFET power switches are switched on and off for half of the fundamental cycle, and the switching loss is determined as follows.

$$P_{SW1} = 2 \times f \times (E_{ON} + E_{OFF}) = \frac{1}{3} \times f \times I\,(V_{ON}T_{ON} + V_{OFF}T_{OFF}) \quad (8)$$

The fundamental switching frequency is f. Similarly, the switching loss of a multi-conversion unit is represented as throughout the half time. It is given by,

$$P_{SW2} = 2 \times f \times (E_{ON} + E_{OFF})f \times I(V_{ON}T_{ON}V_{OFF}T_{OFF}) \quad (9)$$

For a full cycle, the overall switching loss can be deduced as

$$P_{SW,TOTAL} = f \times (P_{SW1} + P_{SW2}) \quad (10)$$

The total power loss and the efficiency of the projected inverter are determined by using (11) and (12)

$$P_{LOSS,,TOTAL} = P_{CON,T} + P_{SW,T} \quad (11)$$

The efficiency has been calculated using the following formulae

$$Efficiency = \frac{P_{OUT}}{P_{out} + P_{LOSS,T}} \times 100\% \quad (12)$$

Table 2. Losses and efficiency.

S.No.	Input Power	Switching Losses	Conduction Losses	Total Losses	Output Power	Efficiency
1	210	0.11	2.76	2.87	207.13	98.62
2	320	0.16	4.58	4.74	315.26	98.51
3	520	0.21	8.22	8.43	511.57	98.38
4	760	0.31	13.01	13.32	746.68	98.25
5	840	0.33	16.37	16.7	823.3	98.01
6	1000	0.35	24.47	24.82	975.18	97.52
7	1200	0.37	33.55	33.92	1166.08	97.17

From the theoretical calculations, the conduction losses of 17 level NRSCMLI is 13.21 W, switching losses of the NRSCMLI is 0.31 W, Input power of the NRSCMLI is 760 W, output power of the NRSCMLI is 746.68W and the efficiency of the NRSCMLI is 98.25%. Losses and efficiency is calculated for input power between 200 W to 1200 W. Table 2 shows the losses and efficiency of proposed MLI for various values of input power. Figure 3 depicts the efficiencies of proposed MLI for various values of input power. From this figure it is clear that efficiency is 97.17 % to 98.62 %.

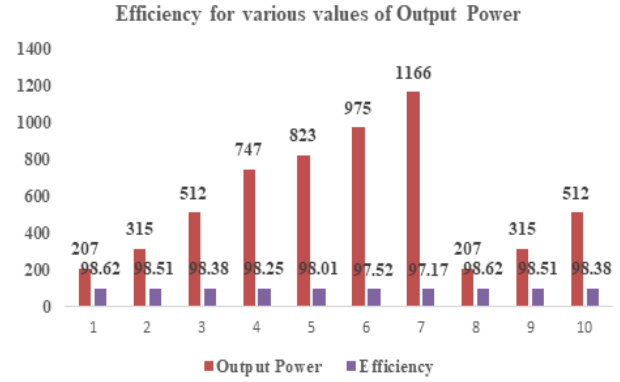

Fig. 3. Efficiency for various input powers.

4. Nearest Level Control for NRSCMLI

NLC is a common approach used in modular multilevel converters. Low switching frequency control technology known as NLC or the round approach is adaptable and simple to use. The semiconductor switches of the converter are activated by the appropriate gating signals produced by the NLC approach. Take the basic sinusoidal function with unit magnitude multiplied by the modulation index as a starting point. Allow the resulting signal to pass through the inverter's total positive levels (N) after that. Employ the round function next to obtain the necessary levels. The round function serves effectively to decrease switching losses by causing just one commutation to occur between two voltage steps, as shown in Fig. 4. Considering a V_{ref}, the modulation index 'm' the nearest voltage level that can be estimated as follows:

$$V_{ref} = \mu\left(\frac{L-1}{2}\right) Vsin(wt) = V_m \sin(wt) \quad (13)$$

$$m = \frac{V_m}{\left(\frac{L-1}{2}\right)V}, V_m = Vround\left(\frac{V_{ref}}{V}\right)$$

V_{ref} - reference sinusoidal voltage

L - number of levels

m - modulation index

V_m – peak ac voltage

V_{dc} – voltage difference between two levels

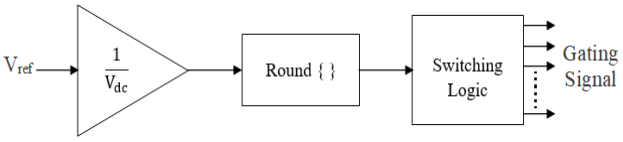

Fig. 4. NLC control method.

Figure 5 shows the production of 17 levels by using NLC.

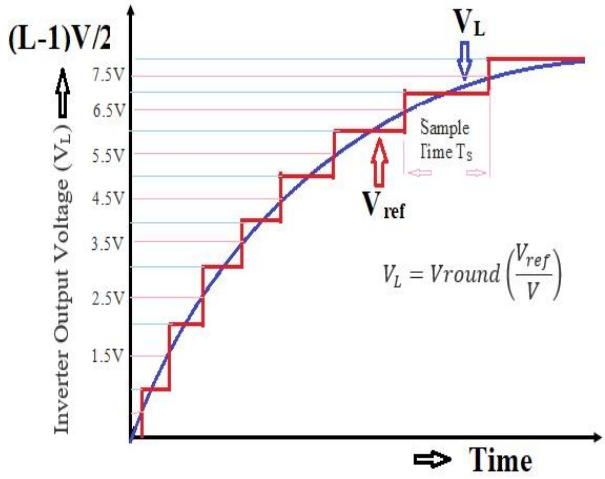

Fig. 5. NLC technique synthesis for 17 level.

5. Results and Discussions

Figure 6 shows MATlab simulation output voltage waveform of 17-level new reduced switch count multilevel inverter. It clearly indicates that the nature of the output waveform is stepped waveform alternate in nature for resistive load of 1kW, the output current waveform is almost sinusoidal waveform for 17 level when it is connected with RL load1 (R=100Ω and L=10mH) and RL load1 (R=150Ω and L=20mH) as

shown in Fig. 7 and Fig. 8. From the Fast Fourier Transform (FFT) analysis window it is realized that while the number of levels are increased, harmonics and total harmonic distortion are reduced. Figure 9 augments for the 17-level inverter, the THD value is 3.43% for R load of 1kW. A simulation result of proposed multilevel inverter is validated with the hardware prototype which comprises of eight power switches. Four MOSFETs (IRF250) are connected to form a multi conversion cell and this is connected with H-bridge which comprises of four MOSFETs. Four asymmetrical DC sources are obtained by using specially designed four separate transformers in the ratio of 1:1, 1:1, 1:2 and 1:4. Input for the all transformer is 28V. Finally, DC voltage is obtained by using rectifiers. A PIC 16F877 microcontroller is used as the foremost processor, which delivers gate trigger signals. With respect to microcontroller control signal MOSFET gate terminal is switched on and off. Inverter output terminal is connected to resistive load and output is measured. The hardware set up is shown in Fig. 10. Hardware output voltage of suggested multilevel inverter is given in figure 11.

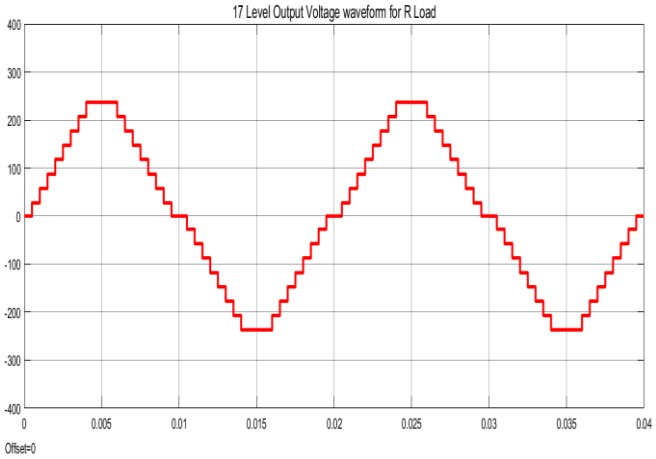

Fig. 6. 17-level output voltage waveform of NRSCMLI for R load.

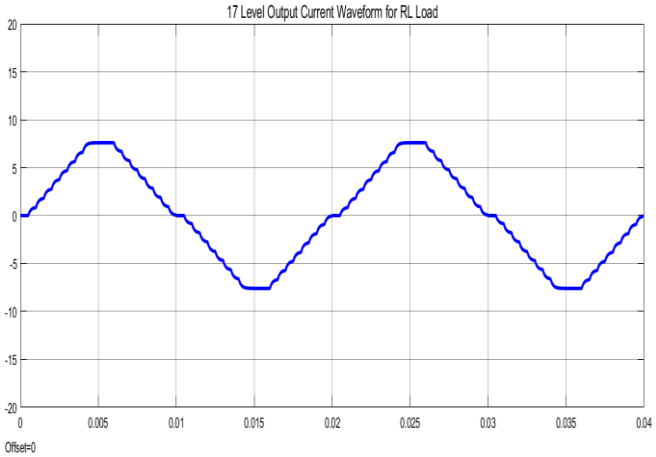

Fig. 7. 17-level output current waveform of NRSCMLI for RL Load1.

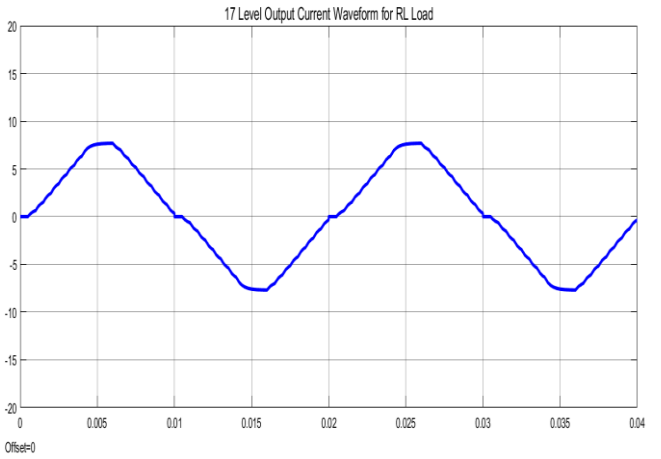

Fig. 8. 17-level output voltage waveform of NRSCMLI for RL load2.

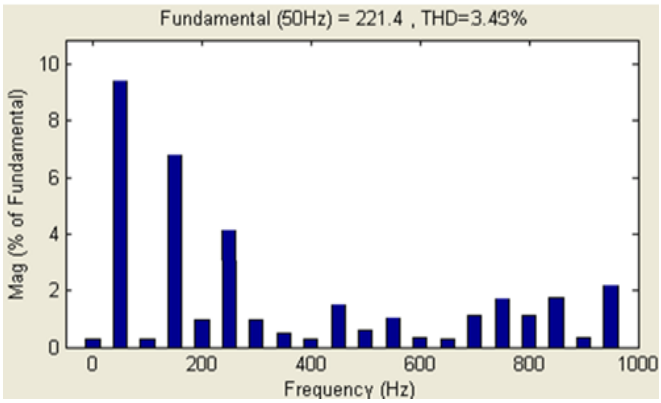

Fig. 9. FFT analysis of 17-level new reduced switch count MLI.

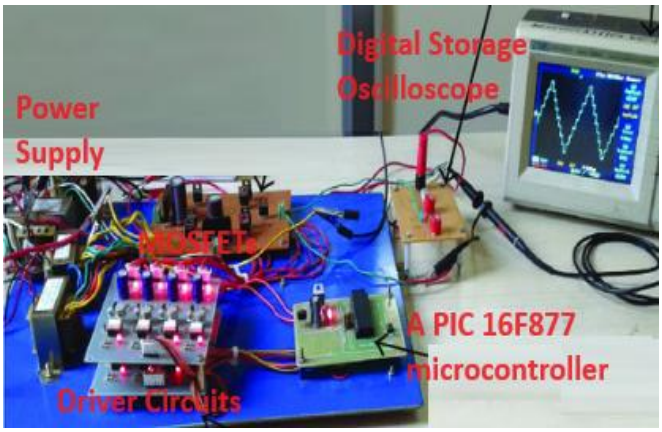

Fig. 10. Experimental Setup.

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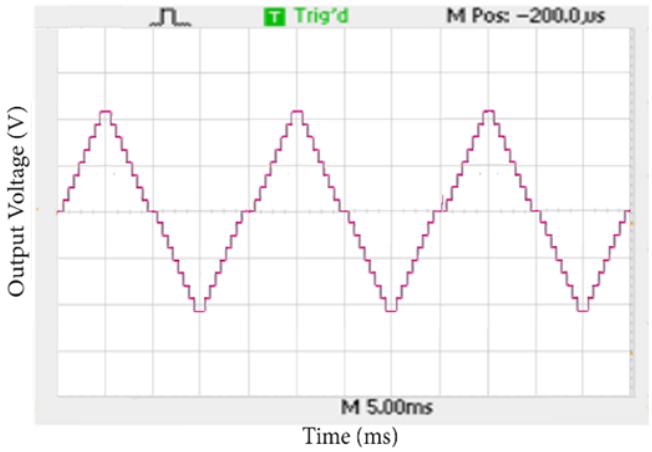

Fig. 11. Hardware output voltage waveform of new reduced witch count MLI.

Figure 12 shows the current waveform of proposed MLI. It clearly shows that both voltage and current waveforms are almost sinusoidal. The resultant output voltage of seventeen level MLI is 224 volts, with 50 Hz frequency. The data from a MOSFET switch with variable output power was used to estimate the efficiency of the suggested configuration. FFT analysis from Fig. 13 shows that THD is 3.82%.

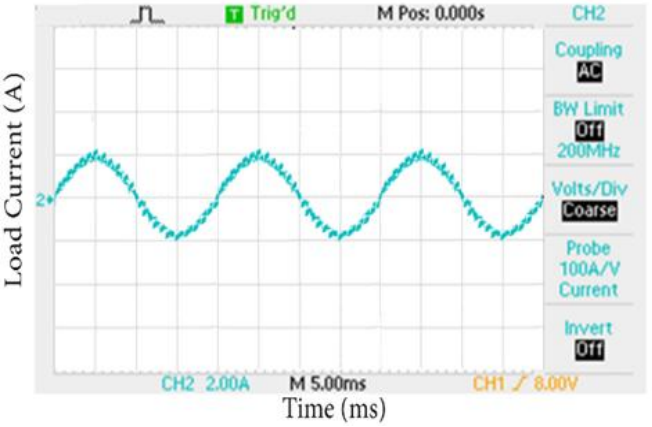

Fig. 12. Hardware output current waveform of new red.uced switch count MLI

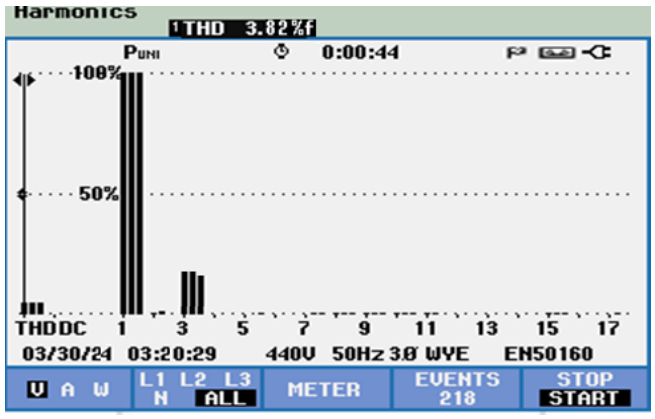

Fig. 13. Hardware FFT analysis of 17-level new reduced switch count MLI.

6. Performance Comparison of Multilevel Inverters

The performance comparison of various MLIs are performed based on the switches, driver circuits, diodes, capacitors, and DC sources used. Total standing voltage, cost function per level, THD and efficiency are compared.

6.1. Calculation of TSV and Cost function

Total Standing Voltage and Cost functions for the proposed MLI are calculated as follows:

$$\text{Total Standing Voltage} = \sum_{i=1}^{n} MBV_{Si} \quad (19)$$

$$TSV = MBV_{S1} + MBV_{S2} + MBV_{S3} + MBV_{S4} + MBV_{S5} + MBV_{S6} + MBV_{S7} + MBV_{S8}$$

$$TSV = 7V_{dc} + 6V_{dc} + 4V_{dc} + 0V_{dc} + 8V_{dc} + 8V_{dc} + 8V_{dc} + 8V_{dc}$$

$$TSV = 49V_{dc}$$

$$TSV_{PU} = \frac{TSV}{MBV} = \frac{49V_{dc}}{8V_{dc}} = 6.12$$

Cost function is given as:

$$CF = (N_S + N_{gd} + N_D + N_C + \alpha TSV_{PU}) \times N_{DC} \quad (20)$$

N_S – No. of Switches
N_{gd} – No. of gate drives
N_D – No. of Diodes
N_C – No. of Capacitors
TSV – Total Standing Voltage
α – Weight co-efficient
N_{DC} – No. of Sources

Cost function is:

N_S =8, N_{gd} = 6, N_D = 4, N_C =0, α =1 and N_{DC} = 4

$$\text{Cost Function} = (8 + 6 + 3 + 0 + 1 \times 6.12) \times 4 = 92.48$$

$$CF/Level = \frac{CF}{\text{Number of Levels}} = \frac{92.48}{17} = 5.7$$

6.2. Comparison with Various MLIs

The several MLI structural topologies are compared conferring to stages accompanying with the quantity of power switches employed. The comparison is made for 17 level based on number of switches, driver circuits, diodes, dc sources, capacitors, TSVpu, CF per level, total harmonics distortion and efficiency. Table 3 shows the comparison of various types of MLIs. Fig. 14 shows the comparison of various existing MLIs based on the

requirement of switches and driver circuits. Figure 15 shows the comparison of TSVpu various existing MLIs. Figure 16 shows the comparison of various existing MLIs based on the diodes, capacitors and DC sources. Figure 17 shows the comparison of various existing MLIs based on TSVpu, CF per level. Figure 18 shows the comparison of various existing MLIs based on THD. it is clear that the suggested topology's efficiency is 98.24% and TSV is 6.12. The new reduced switch count MLI has benefits of 17 levels with only 8 numbers of power switches when multisource is utilized, THD is 3.43 % and efficiency is also high when compared to various multilevel inverters. In this proposed MLI, 4 DC sources are used to generate 17 levels output whereas in conventional inverters minimum 4 DC sources required otherwise one or two sources with more capacitors are required to generate the same 17 levels. With the usage of more capacitors, voltage balancing issues may arise. From the comparison, it depicts that the developed MLI is best suited for electric vehicle applications with low number of power switches, reduced THD and more efficiency. From these above calculations, cost function per level is less when compare to conventional topologies.

Table 3. Evaluation of Multilevel Inverters with Respect to Different Configurations.

S.No.	Name of the Topology	Switches	Driver Circuits	Diodes	Capacitors	DC Sources	TSVpu	CF α=0.5	CF α=1	THD	Efficiency (%)
1	DCMLI	16	16	14	8	1	32	4.1	5.1	7.53	96.81
2	FCMLI	16	16	0	18	1	32	3.9	4.8	7.12	96.52
3	CHBMLI	32	32	0	0	8	4	31.1	32	7.81	95.75
4	CHBHMLI	12	12	0	0	3	6	4.8	5.3	7.1	97.10
5	NCMLI	20	18	0	0	8	11	20.5	23.1	7.44	96.21
6	NCHMLI	12	10	0	0	4	8.25	6.1	7.1	5.51	97.12
7	MCMLI	12	10	8	0	8	7.5	15.9	17.6	6.26	96.88
8	[31]	11	11	1	3	1	7.00	1.74	2.15	7.19	96.30
9	[32]	24	24	2	4	3	9.00	10.32	11.91	6.50	97.89
10	[33]	14	14	4	4	1	7.50	2.34	2.78	5.72	94.50
11	[34]	11	11	2	1	2	6.75	3.34	4.13	5.89	97.70
12	[35]	14	14	2	4	2	5.67	5.67	6.54	7.45	91.00
13	Proposed MLI	8	6	4	0	4	6.12	5.0	5.7	3.43	98.24

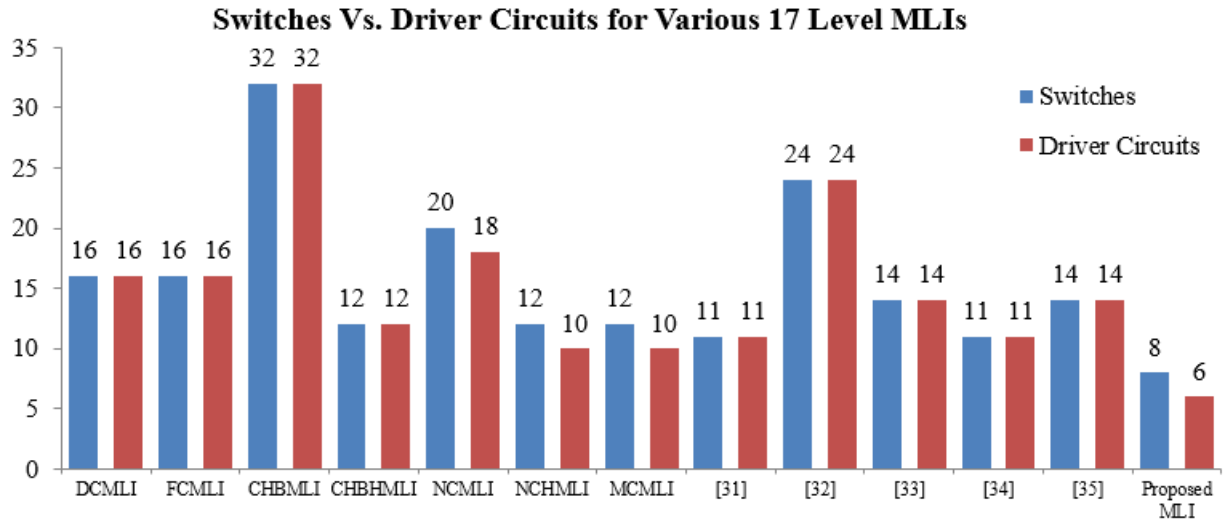

Fig. 14. Comparison of Various Existing MLIs- Switches vs. Driver Circuits.

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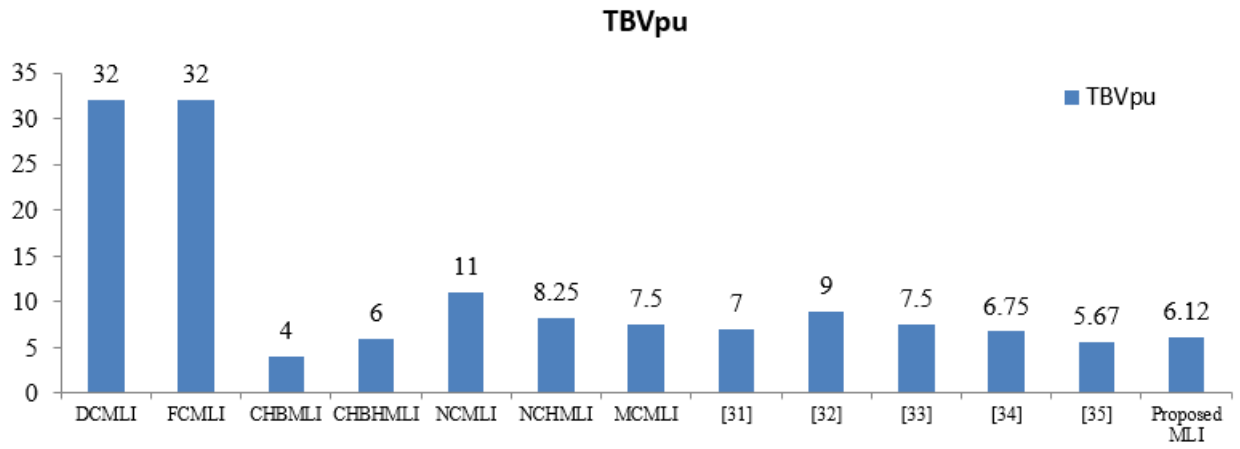

Fig. 15. Comparison of Various Existing MLIs based on TSVpu.

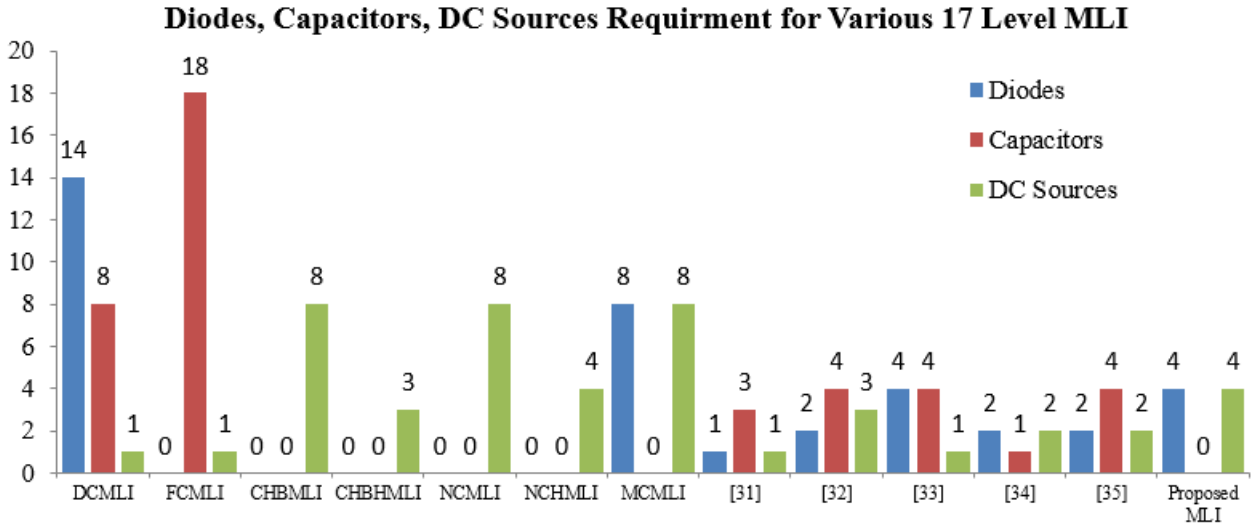

Fig. 16. Comparison of Various Existing MLIs based on diodes, capacitors and DC sources required for 17 levels.

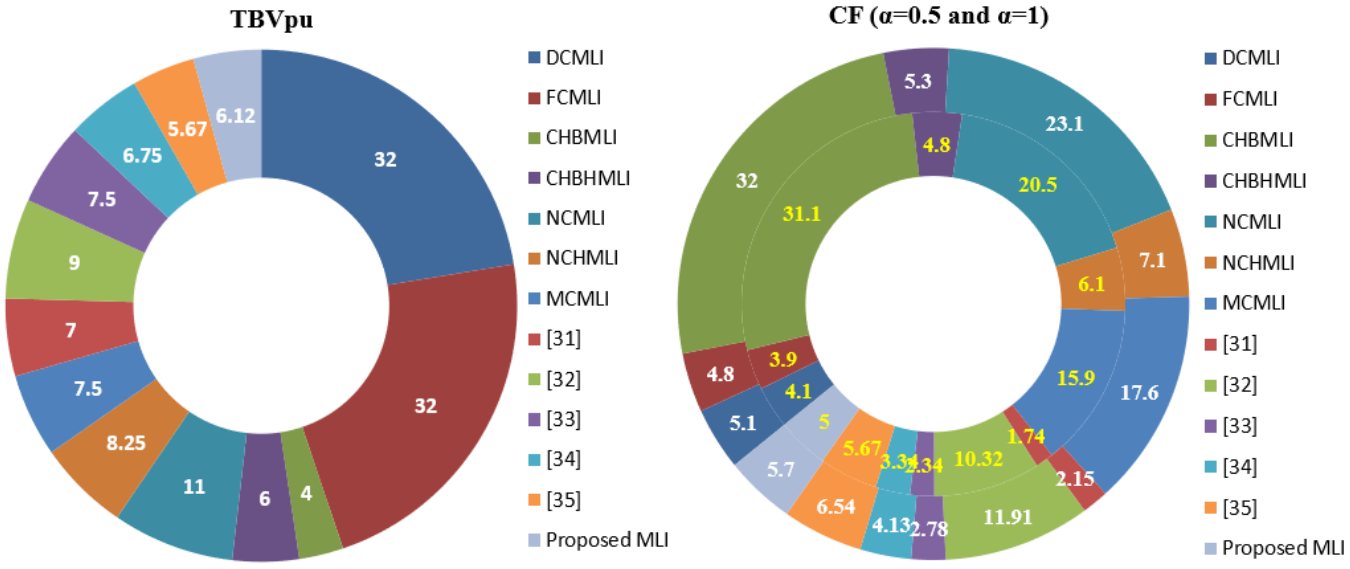

Fig. 17. Comparison of Various Existing MLIs based on TSVpu, CF per level for 17 levels.

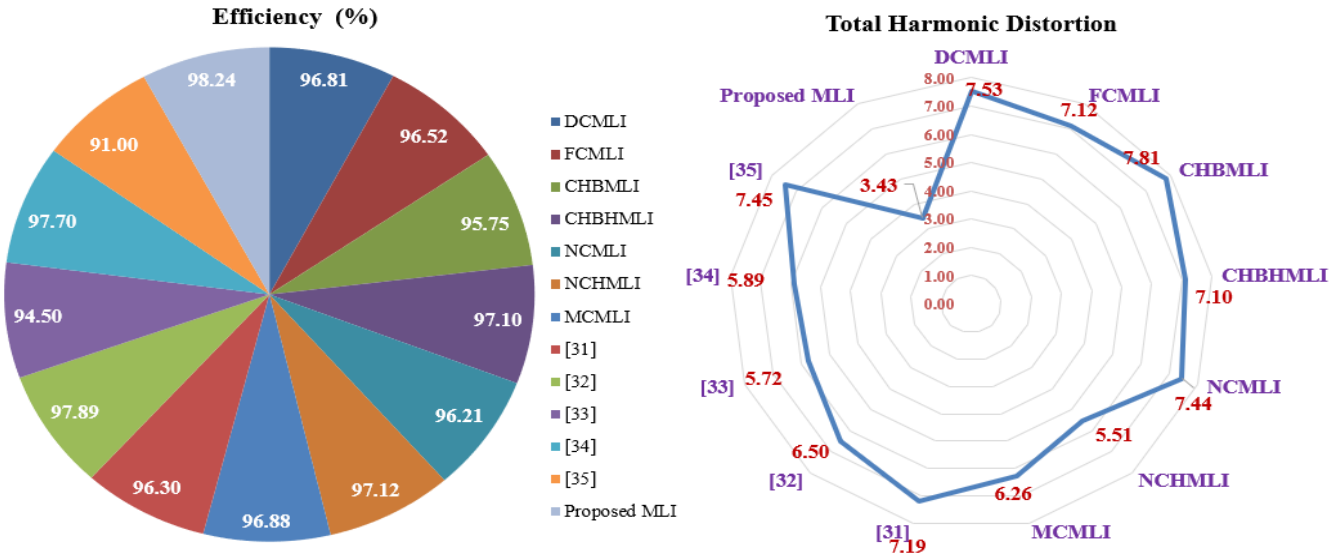

Fig. 18. Comparison of Various Existing MLIs based on efficiency and THD for 17 levels.

7. Conclusion

The need for high energy-based efficient converters has grown as a result of the development and improvement of various sectors and academic research worldwide. Due to their inherent advantages, MLIs have become quite popular and are used in DC/AC conversion processes for high/medium voltage and high-power applications. In this regard, A seventeen level MLI is proposed and results have been validated in both simulation and hardware setup. The different multilevel inverter structures and its basic operations have been discussed. The mathematical expressions for the calculation of required voltage level at the load side on each stage has been pronounced. A detailed comparison has been done based on the number of switches, driver circuits, diodes, capacitors, and DC sources required for generating 17 level output. Comparison also has been done for TSV per unit, THD, Cost function per level. In the conservative approaches, as the number of levels are increased, the essential numbers of power switches have also been increased. Due to the engrossment of large count of power switches, the harmonics, total harmonics distortion, switching losses, and the implementation cost are also increased. The suggested topology considerably reduces the power switches to 8 for 17 levels which will lower the losses due to switching, lower order harmonics, costs and leads to improvement in reduced Total Harmonics Distortion and increased efficiency. Hence, the proposed MLI is best suited for electric vehicle and other applications.

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