

*Article*

## A Zero Bias Pixel Sensor and its Zero-Bias Column Buffer-Direct-Injection Circuit

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**Abstract.** Two pixel sensors, namely active pixel sensor (APS) and pseudo-active pixel sensor (PAPS), are reviewed to show that APS suffers from dark current while PAPS suffers from leakage current. Then a new pixel sensor called zero bias pixel sensor (ZBPS) in which only two MOS switches in addition to the photodiode are used, one for connecting the pixel's photodiode to a column bus and the other for bypassing it. A zero-bias column buffer-direct-injection (ZCBDI) circuit, which is similar to a regulated cascode amplifier, is used to control the voltage at column bus at zero. All ZBPS pixels are guaranteed to work at zero voltage at all times to eliminate the dark current as well as leakage current. A case of a  $10\mu\text{m} \times 10\mu\text{m}$  ZBPS pixel designed with standard  $0.18\mu\text{m}$  CMOS process is studied through simulation. This pixel generates a photocurrent within a range from  $1\text{pA}$  to  $100\text{nA}$ . To handle a large variation of photocurrent while maintaining zero column voltage, the ZCBDI is designed using differential cascode, common source, and buffer stages and then compensated for 50 degree phase margin. Transient simulation shows that the pixel steady state response time is around  $1.406\text{ms}$ , leading to at most 5.5 frames per second for an image of  $128 \times 128$  ZBPS pixels. The fill factor of ZBPS for this case is around 59%.

**Keywords:** CMOS sensor, zero bias pixel, dark current.

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## 1. Introduction

A CMOS image sensor as shown in Fig. 1(a) is a device that converts light from an object into electrical signal so that its image can be captured and stored in digital form. It is found in many consumer products such as digital camera, smart phone, and medical imaging equipment [1-4]. The general structure of a CMOS image sensor is shown in Fig. 1(b) where a major portion of the chip area is occupied by an array of pixels. All pixels in the same column share their output and all pixels in each row are selected by activating a row select control which connects them to their respective column readout for further processing. A pixel consists of a photodiode, a select switch and other interface (if any) as shown in Fig. 1(c). For maximum sensitivity [5, 6], the photodiode should occupy the largest proportion of the total pixel area or “fill factor”. With today advance technology, it is common to find a CMOS image sensor having as array of 1,000x1,000 or 1 million pixels, each of which has a size less than  $10\mu\text{m} \times 10\mu\text{m}$ .

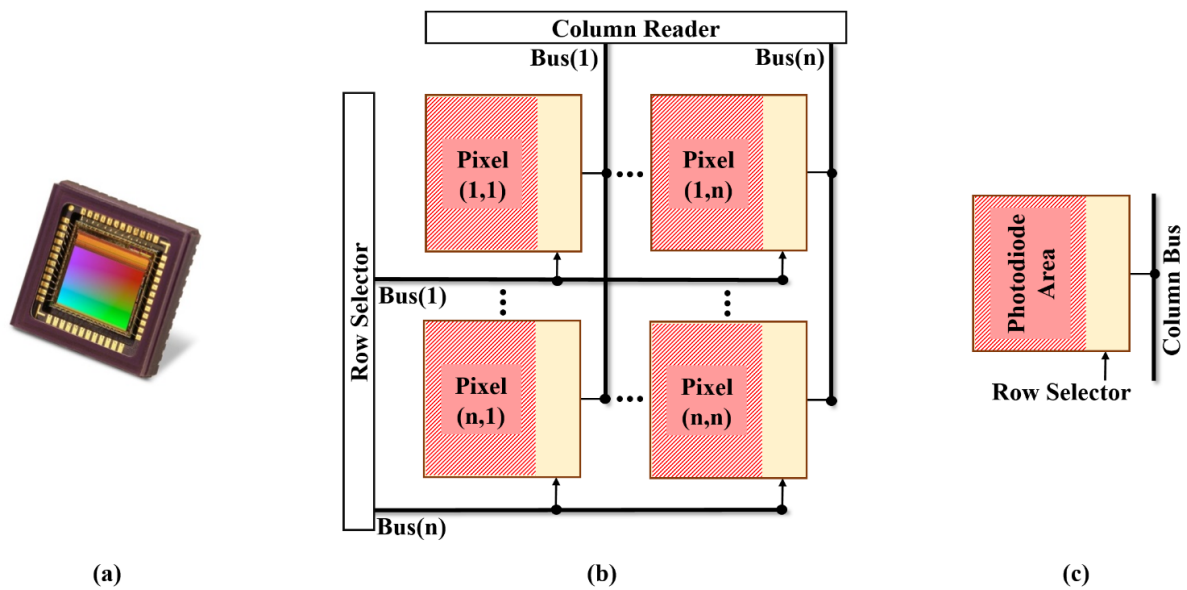


Fig. 1. (a) CMOS image sensor [7]; (b) array of pixels; (c) pixel structure.

Fig. 2 shows the symbol of a photodiode and its characteristic curves. Physically, a photodiode consists of a junction of p and n type semiconductor layers [8]. When exposed to light, electron-hole pairs are generated in the junction’s space charge region and driven out by the electric field from the applied bias voltage  $V_{ph}$ , generating a photocurrent  $I_p$  that is proportional to the light intensity  $P$  and the bias voltage. At the same time, the bias voltage  $V_{ph}$  also causes an additional current, called “dark current” or  $I_{dark}$ , due to tunneling and SRH generation [9, 10]. Therefore the output current  $I_{ph}$  of the photodiode is the sum of photocurrent  $I_p$  and dark current  $I_{dark}$ . Note that dark current disappears when the photodiode is operated at zero voltage.

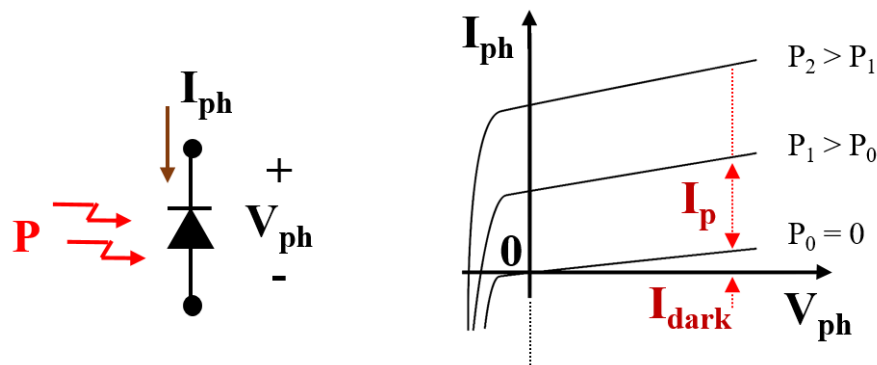


Fig. 2. Symbol of a photodiode and its current vs. voltage characteristics (not to scale).

This paper focuses on a pixel structure that produces low dark current since it not only degrades optical dynamic range, but also contributes noise [9, 11, 12]. In particular, 2 types of pixel structure are reviewed. They are active pixel sensor (APS) [6, 13-25] in Section 2 and pseudo-active pixel sensor (PAPS) [26, 27] in Section 3. Then a new sensor called zero bias pixel sensor (ZBPS), that can eliminate dark current, is proposed in Section 4. Since ZBPS requires a zero-bias column buffer-direct-injection (ZCBDI) circuit to control the column bus at zero voltage, a design case of ZCBDI capable of supporting 1pA to 100nA of photocurrent is described in Section 5. Section 6 finishes the design with frequency compensation for stability along with transient simulation studied in Section 7 which characterizes the achieved frame rate. Conclusion is then discussed in Section 8.

## 2. Active Pixel Sensor (APS)

The most common CMOS pixel sensor is the active pixel sensor (APS) [6, 13-25] which has 2 conventional types, namely 3T APS [6, 14, 18, 21-24] and 4T APS [13-20, 25], as shown in Fig. 3. Both types use the junction capacitor of a photodiode to integrate its current and measure the change in its voltage after a fixed time interval which depends linearly on the incident light intensity. The 3T APS uses 3 MOS transistors and can be fabricated in a standard low cost CMOS process but suffers from dark current and reset noises [9, 11, 12]. The more popular 4T APS uses 4 MOS transistors and replaces the photodiode with a “pinned” photodiode [13] which inherently has lower dark current but requires special fabrication steps. The fill factor is usually around 40% for 3T APS and 30% for 4T APS.

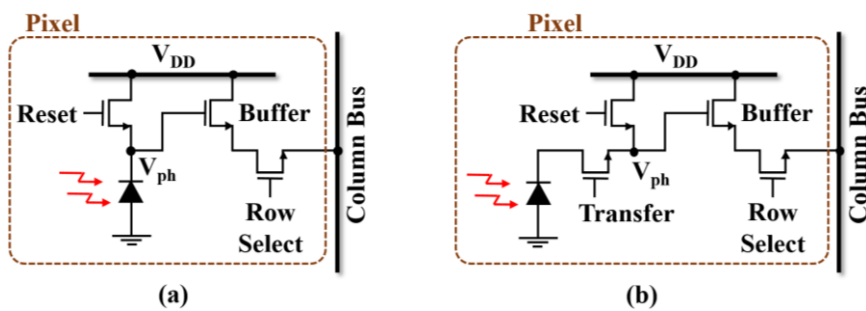


Fig. 3. (a) 3T active pixel sensor; (b) 4T active pixel sensor.

The light conversion of 3T APS is described with the help of Fig. 4 as follows. First, a pixel is reset, as seen in Fig. 4(a), so that its junction capacitor  $C_j$  is charged by the DC supply  $V_{DD}$ . Then the reset switch is off and the pixel capacitor is discharged by its photocurrent and dark current, as seen in Fig. 4(b), causing its voltage to ramp down, i.e.

$$V_{ph}(t) = V_{DD} - \frac{1}{C_j} \int_0^t (I_p + I_{dark})(t) dt \quad (1).$$

At the end of the integration time  $T$ , typically in the order of milliseconds, the voltage of the selected pixel is readout by the buffer to the column bus as depicted in Fig. 4(c). Then the pixel goes back to a new cycle. Note that APS pixel cannot reduce or eliminate dark current, although 4T APS replaces the normal photodiode by a pinned photodiode which has lower dark current [28].

## 3. Pseudo-Active Pixel Sensor (PAPS)

One pixel structure that can reduce dark current of photodiode is proposed in [26]. It is called pseudo-active pixel sensor or PAPS. Fig. 5 depicts two types of PAPS based on whether the photodiode is implemented from p+/n-well (left) or n-well/p-substrate (right). Unlike APS, the output of PAPS is the photocurrent, not integrated voltage. The basic idea of PAPS is to operate the selected pixel at zero voltage to eliminate its dark current and allow only photocurrent to flow out of the pixel. This zero voltage is accomplished by a circuit called zero-bias column buffer-direct-injection or ZCBDI (see Fig. 5) which is

shared by all pixels in the same column. It consists of an operational amplifier for zero biasing and a buffer PMOS or NMOS for injecting the photocurrent to charge a column capacitor  $C_{int}$  which was initially discharged (Fig. 5 left) by the reset switch. After a fixed integration time  $T$ , the capacitor voltage is readout and is given by

$$V_{int}(T) = \frac{1}{C_{int}} \int_0^T I_{int}(t) dt \tag{2}$$

Note that the column bus is hold by ZCBDI at  $V_{DD}$  for the left PAPS and zero for the right PAPS. Since a PAPS needs only one select switch, its fill factor can be high. For example, the fill factor of a  $5.8\mu\text{m} \times 5.8\mu\text{m}$  PAPS pixel size can reach 58%.

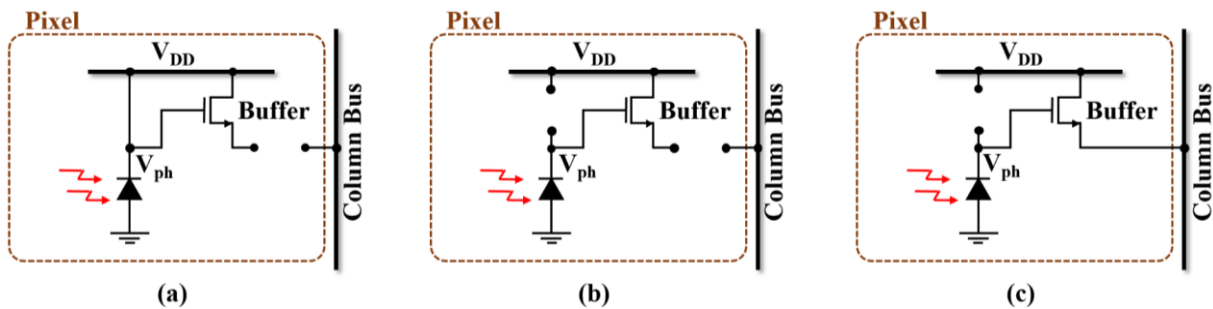


Fig. 4. Operation of 3T APS during (a) reset, (b) integration and (c) readout phase.

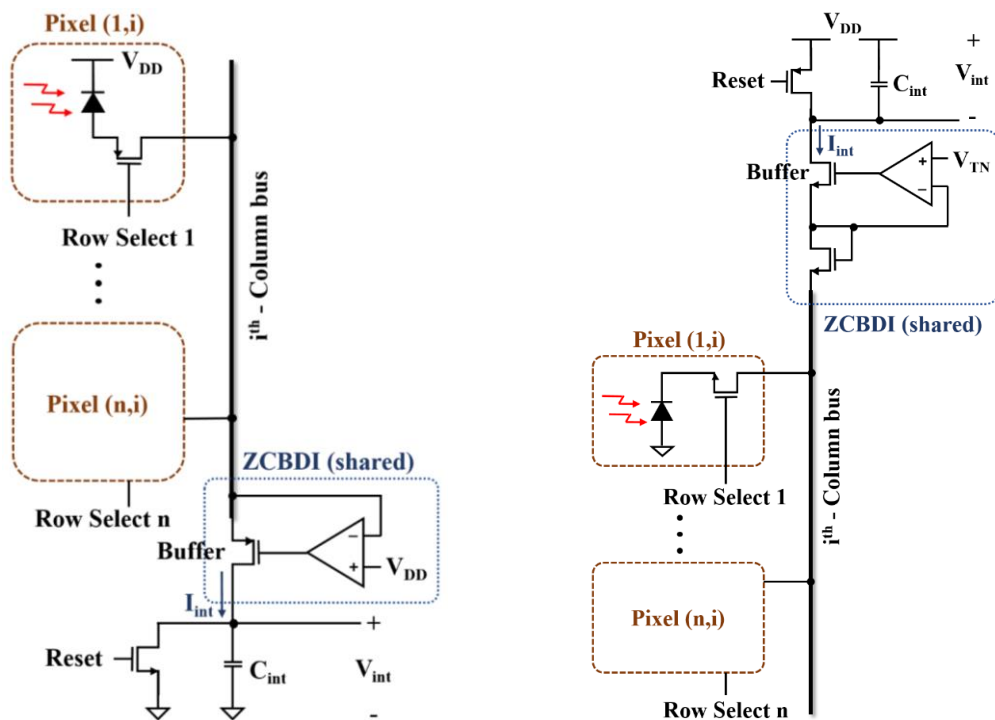


Fig. 5. PAPS using p+/n-well (left) and n-well/p-substrate (right) photodiodes.

Since any unselected PAPS pixel is not connected to the column bus, its photocurrent causes a forward self bias voltage  $\delta$  (see Fig. 6) of a few hundred millivolt. This voltage can produce a leakage current  $I_{leak}$  through its own select switch to the column bus as shown in Fig. 6. Therefore the current  $I_{int}$  that is injected into the integrating capacitor is equal to the photocurrent of the selected pixel plus the sum of leakage currents of all unselected pixels in the same column. Although each leakage current is only a tiny fraction of the photocurrent, its effect becomes pronounced when there is a large number of pixels

connected to a column. In [27], it is suggested that one ZCBDI should be shared with only 4 PAPS pixels, called OPAPS. This results in using more than one ZCBDI per column and effectively reduces the fill factor down to 42% for a 352x288 pixel array. Also since the photocurrent decreases with the reverse bias voltage, its value is smaller than that of APS.

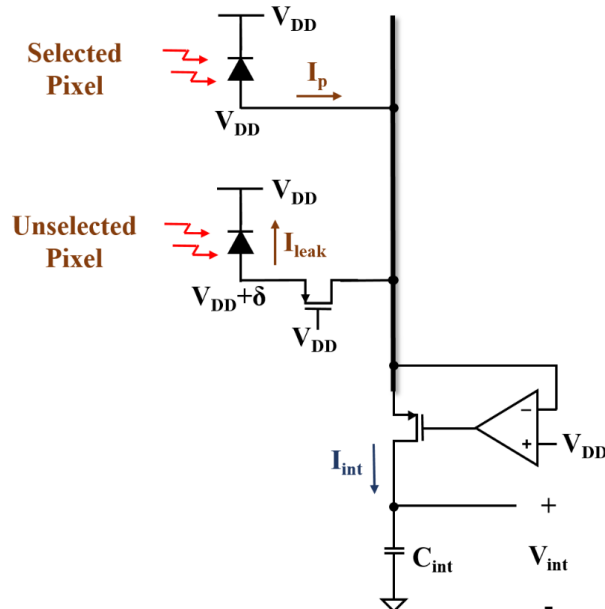


Fig. 6. Operation of PAPS during integration.

#### 4. Zero Bias Pixel Sensor (ZBPS)

To eliminate leakage currents from unselected PAPS pixels, a bypass switch is added across each photodiode as shown in Fig. 7(a). In this new structure, a selected pixel is zero biased by ZCBDI while unselected pixels are bypassed as shown in Fig. 7(b). Using this technique, all pixels are always be zero biased and the pixel sensor is thus called “zero bias pixel sensor” or ZBPS. With no leakage, there is no limit on the number of pixels connected to a column which is an advantage over PAPS. Note also that there is a slight difference in designing ZCBDI between ZBPS (Fig. 7) and PAPS (Fig. 5). The disadvantage of ZBPS is that its fill factor tends to lower than PAPS. As an example, a  $10\mu\text{m} \times 10\mu\text{m}$  ZBPS design is shown in Fig. 8. Its fill factor is 59% which is comparable of PAPS in [26] (with pixel size almost 4 times bigger) but larger than 42% of OPAPS in [27].

#### 5. A Circuit Design of a ZCBDI

Designing ZCBDI is challenging because it has to handle photocurrent of 5 order of magnitude variation. Also there is a stability issue with the circuit since it employs a feedback loop to control the column at zero voltage. Here we present a design case where a pixel generates 1pA at low light condition and 100nA at full light intensity. Its size is  $10\mu\text{m} \times 10\mu\text{m}$ , using  $0.18\mu\text{m}$  CMOS process with the following parameters.

Electron mobility factor  $\mu_n C_{OX} = 200\mu\text{A}/\text{V}^2$

Threshold voltage  $V_{TH} = 0.47\text{V}$

p-n saturation current  $I_S = 210\text{aA}$

Minimum width  $W_{min} = 0.22\mu\text{m}$

Minimum length  $L_{min} = 0.18\mu\text{m}$

The DC supply voltage is 1.8V

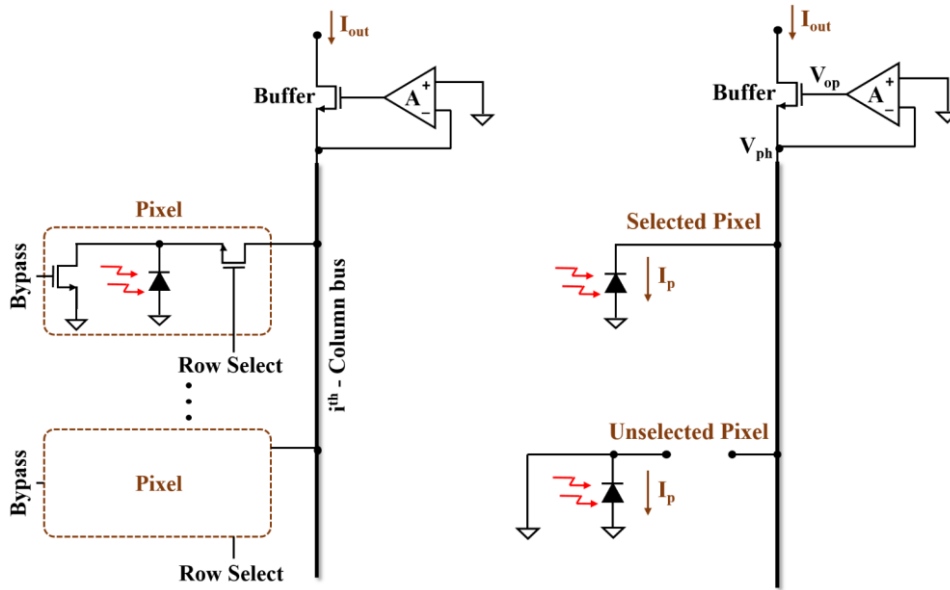


Fig. 7. (a) ZBPS structure; (b) Operation of selected and unselected ZBPS.

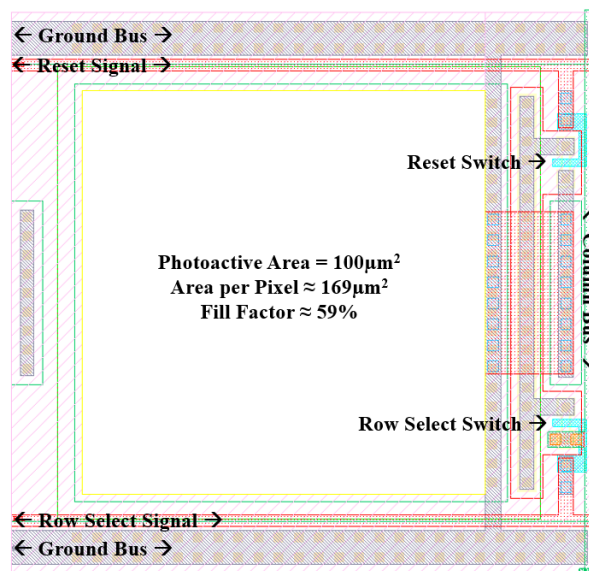


Fig. 8. Layout of a 10µm x 10µm ZBPS.

It is clear from Fig. 7 that the gain of the operational amplifier, A, should be large to make the bias voltage,  $V_{ph}$ , approach zero. Since the operational amplifier drives the gate of the buffer, its output voltage,  $V_{op}$ , should have a high swing to enable the buffer to carry a large variation of photocurrent from 1pA to 100nA. With these observations, the operational amplifier is designed to have two cascaded stages as shown in Fig. 9. The first stage is a high gain folded cascode amplifier [29] and consists of MN11-MN14 and MP11-MP14. The second stage, consisting of MN21 and MP21, is a common source amplifier with a high swing for driving the buffer. Analytically, the gain of the folded cascode amplifier is

$$A_{cascode} = g'_{mp12} r'_{op14} \tag{3}$$

$$g'_{mp12} = g_{mp12} \frac{R_{on12}}{R_{on12} + 1/g_{mn13}} \approx g_{mp12} \tag{4}$$

$$r'_{op14} \approx r_{op14} \parallel (r_{op12} g_{mn14} r_{on14}) \approx r_{op14} \tag{5}$$

where  $g_{mx}$ ,  $r_{ox}$  are transconductance and output resistance of Mx transistor respectively.

Similarly the gain of the common source amplifier is

$$A_{c-source} = -g_{mp21}(r_{op21} \parallel r_{on21}) \quad (6)$$

The total gain is  $A=A_{cascode} \times A_{c-source}$ . Note that the values of  $g_{mx}$ ,  $r_{ox}$  depend not only on MOS sizes but also on the DC operating point which, in turn, depends on the photocurrent. Therefore the designed circuit of Fig. 9 will be verified for two extreme values of photocurrent, i.e. 1pA and 100nA. Since all MOS are of short channel type, exact formula for determining  $g_{mx}$ ,  $r_{ox}$  can only be obtained by numerical simulation. Thus the design procedure starts with choosing initial values of MOS size and iteratively adjusting them until the simulation result yields satisfactory results. After several iterations, the appropriate size of all MOS and DC sources are tabulated in Table 1. DC quiescent values at various photocurrents are tabulated in Table 2 which shows that the designed ZCBDI circuit can vary the amplifier output  $V_{op}$  wide enough the keep the bias voltage  $V_{ph}$  very close to zero.

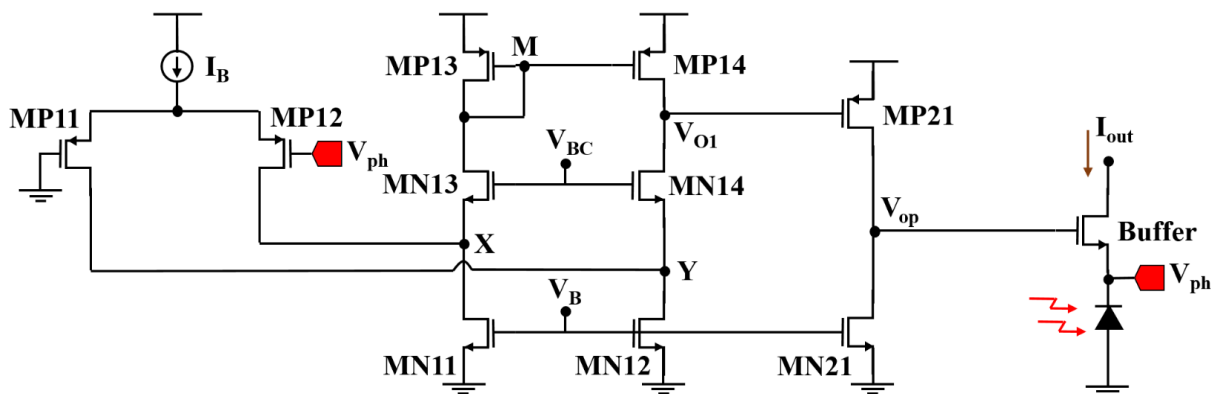


Fig. 9. Schematic diagram of a ZCBDI.

Table 1. MOS sizes and biases of the ZCBDI designed in Fig. 9.

Component	W/L or Value
MP11, MP12, MP13, MP14, MP21	2 $\mu$ m/20 $\mu$ m
MN11, MN12, MN13, MN14	2 $\mu$ m/60 $\mu$ m
MN21	1 $\mu$ m/60 $\mu$ m
Buffer	0.22 $\mu$ m/120 $\mu$ m
$I_B$	100nA
$V_{BC}$	1.0V
$V_B$	0.7V

Table 2. DC operating values of the designed ZCBDI at various photocurrent.

$I_{ph}$	$V_{ph}$	$V_{op}$
1pA	1.8 $\mu$ V	172mV
10pA	220nV	259mV
100pA	88nV	359mV
1nA	29nV	492mV
10nA	-50nV	720mV
100nA	-252nV	1.31V

From Table 2,  $V_{ph}$  is indeed very small as desired but turns out to be slightly negative at large photocurrent. This can be explained as follow. From the operational amplifier characteristic, we have



$$V_{pb} = \frac{V_{op0} - V_{op}}{A} \quad (7).$$

where  $V_{op0}$  is the output voltage at the DC condition when the two inputs of the operational amplifier are equal to zero, therefore,  $V_{op0}$  is not zero in this case. From the buffer MOS transistor, we have

$$V_{pb} = V_{op} - V_{gs}(I_{pb}) \quad (8).$$

where  $V_{gs}$  is the gate source driving voltage which depends on  $I_{ph}$ . Solving these two relations, we obtain

$$V_{pb} = \frac{V_{op0} - V_{gs}(I_{pb})}{1 + A} \quad (9).$$

Therefore  $V_{ph}$  goes to zero when  $A$  is large. However,  $V_{gs}$  increase with  $I_{ph}$ , although nonlinearly. Thus  $V_{ph}$  can be negative when  $I_{ph}$  is large, i.e. 10nA and 100nA for this design. This effect can be reduced by making the buffer MOS bigger.

## 6. Stability and Compensation of the ZCBDI Circuit

Despite having good property in keeping  $V_{ph}$  at almost zero in steady state DC situation, the ZCBDI circuit is susceptible to transient instability because it has a negative feedback path from the pixel to the input of the operational amplifier. Stability is determined from the phase margin obtained from the frequency response of the loop gain,  $A_{loop}$ , which is equal to the product of the gains of the cascode stage, output stage and current buffer stage. Due to different small signal characteristics since different quiescent point at each photocurrent value, its magnitude and phase vary with frequency. Fig. 10 depicts a simulated 1mHz - 1MHz frequency response plot of the loop gain of the ZCBDI of Fig. 9 at two extreme pixel currents, i.e. 1pA and 100nA. From these graphs, the frequency at which the magnitude of the gain is 1 or  $f_{UG}$  is found to be 5.94kHz and 227kHz and the phase margin at  $f_{UG}$  is 12 and -164 degree respectively.

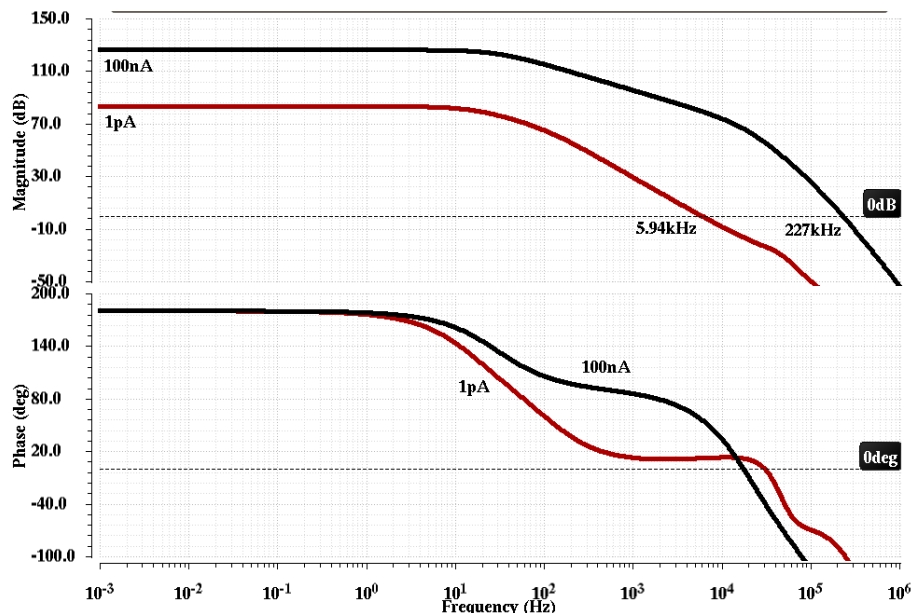


Fig. 10. Frequency response of the loop gain of uncompensated ZCBDI at 1pA and 100nA pixel current.

A common technique to increase the phase margin is to shift the dominant pole to the origin and cancel some of the other poles by adding zeroes in the gain function. This is implemented by adding compensating components  $R_Z$ ,  $C_C$  and  $C_Z$  to the ZCBDI of Fig. 9. The result is shown in Fig. 11. The need



for  $C_C$  is to exploit its Miller effect to lower the dominant pole of the magnitude plot which occurs at node O1. It can be approximated to be

$$\text{Dominant pole} \approx -\frac{1}{r_{op14}'(C_{O1} + (1 + A_{e-source})C_C)} \quad (10)$$

where  $C_{O1}$  is the parasitic node capacitance. Other components  $R_Z$  and  $C_Z$  create zeroes at

$$-\frac{g_{mp21}}{(g_{mp21}R_Z - 1)C_C} \quad (11)$$

and

$$-\frac{g_{mbuffer}}{C_Z} \quad (12).$$

These zeroes improve the phase margin by cancelling the effect of non-dominant poles. Through iterations, a good choice of these components is found to be  $R_Z = 4.1M\Omega$ ,  $C_C = 1pF$  and  $C_Z = 0.5pF$ . The loop frequency plot of this compensated ZCBDI is depicted in Fig. 12 giving 50 and 70 degree of phase margin at 1pA and 100nA photocurrent. These margins are sufficient to guarantee stability.

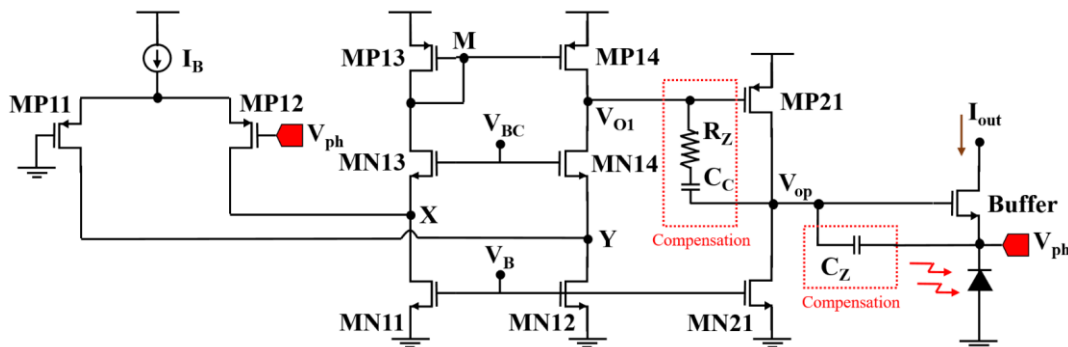


Fig. 11. ZCBDI using  $R_Z$ ,  $C_C$  and  $C_Z$  as compensating components.

## 7. Transient Response of the Compensated ZCBDI Circuit

Once stabilized, the transient simulation of the compensated ZCBDI in Fig. 11 is carried out. Here the  $I_{ph}$  changes stepwise only from 50pA to 50nA corresponding to typical 50 lux to 50,000 lux ambient condition thereby yielding 10 bits of digitization resolution. Although the main function of ZCBDI is to control the pixel bias voltage at zero, it also has to accurately buffer  $I_{ph}$  to  $I_{out}$ . Therefore the settling time or  $T_s$  is determined from considering on  $I_{out}$  (time for  $I_{out}$  to reach within  $\pm 5\%$  of the steady value) instead of  $V_{ph}$ . Careful derivation of the small signal analysis shows that this settling time is approximately proportional to  $I_{ph}$ , although the exact value is difficult to determine from such a large signal transition. Fig. 13 shows the transient waveform with  $I_{ph}$  varies from 50pA to 50nA giving 15 $\mu$ s settling time, whereas Fig. 14 shows the response of step  $I_{ph}$  from 50nA to 50pA with a much longer settling time of 1.406ms. Note that the waveform of  $V_{ph}$  experience ringing behavior which indicates that the phase margin of the loop is not large enough to suppress the ringing. Since  $T_s$  is the time to process one row of pixels, the frame rate to capture an array of  $N_{rows} \times N_{column}$  of pixels is then given by

$$\text{Frame rate} < \frac{1}{N_{rows} \times T_s} \quad (13)$$

where  $T_s$  is the longest settling time. Therefore the frame rate of a 1000x1000 pixels is 0.7 frames per second and of a 128x128 pixels is 5.5 frames per second. This figure indicates that the designed ZCBDI is suitable for taking still pictures, not video.

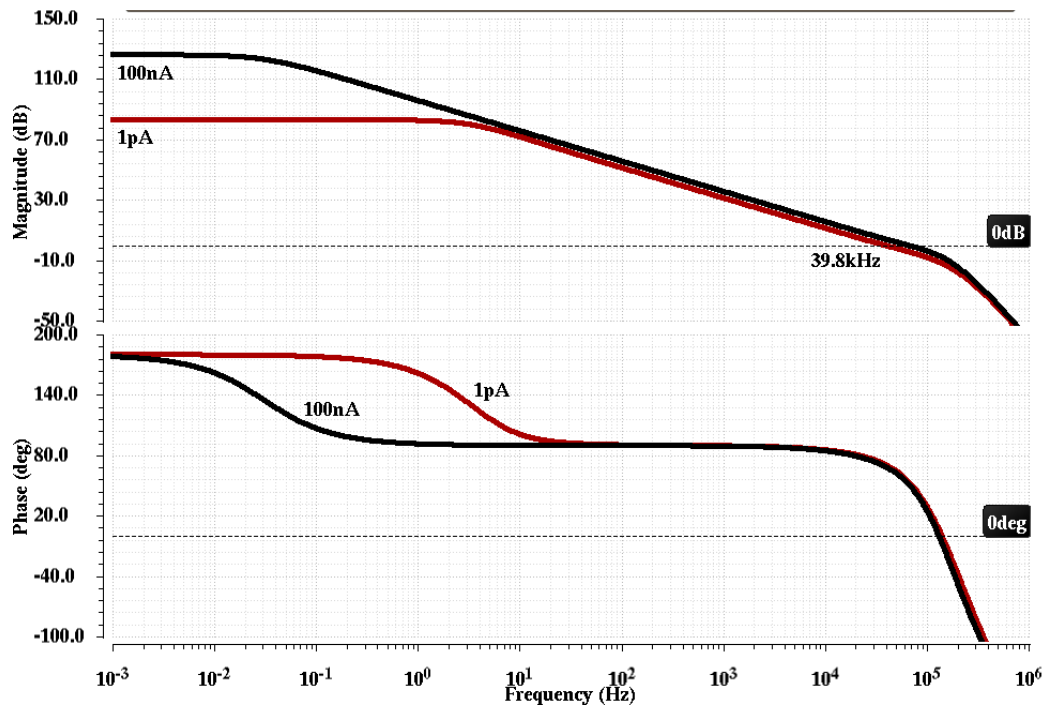


Fig. 12. Frequency response of the loop gain of compensated ZCBDI.

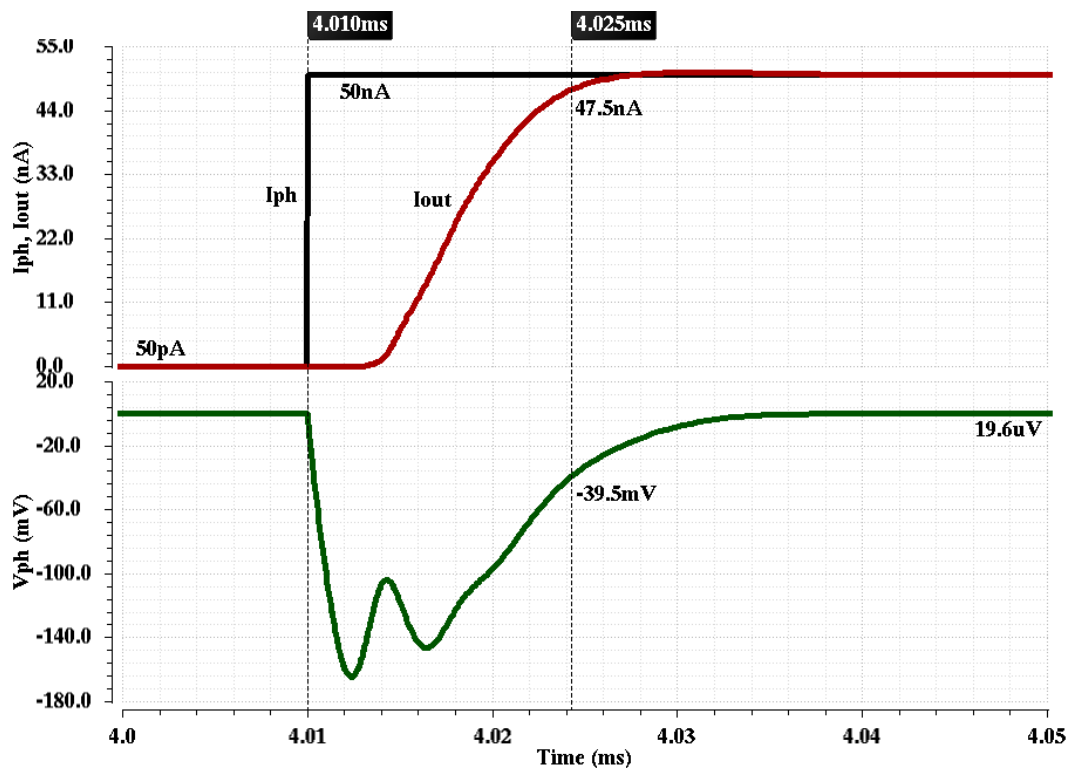


Fig. 13. Transient response of the compensated ZCBDI for a 50pA to 50nA step of photocurrent.

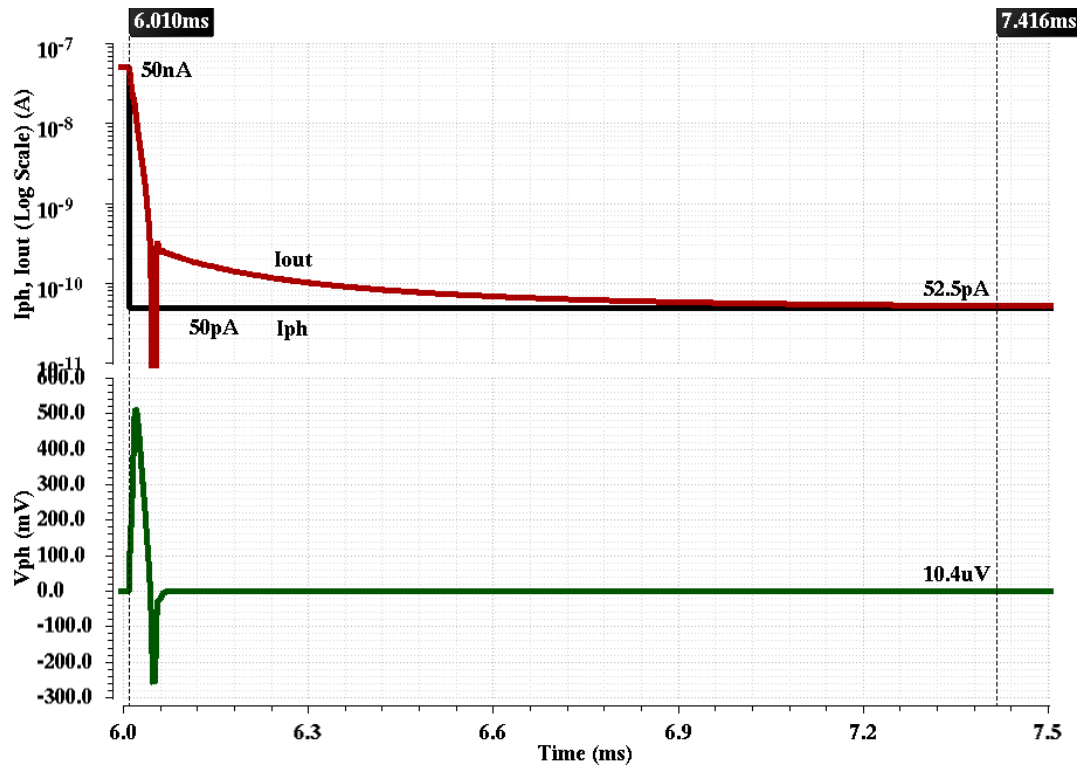


Fig. 14. Transient response of the compensated ZCBDI for a 50nA to 50pA step of photocurrent.

## 8. Conclusion

Operating a photodiode at zero voltage can completely eliminate its dark current. This has led to a new pixel called zero bias pixel sensor (ZBPS) in which all pixels are always biased at near zero voltage. A ZBPS structure requires 2 MOS transistors in addition to the photodiode, one for select and the other for bypass. The basic idea is to bypass unselected pixels while connecting the selected one to a column bus that is hold at zero voltage by a shared regulated cascode amplifier called ZCBDI. This new sensor has the lowest dark current when compared with APS and PAPS. The conceptual and detailed design of the ZCBDI for a  $10\mu\text{m} \times 10\mu\text{m}$  pixel in a  $0.18\mu\text{m}$  CMOS process that is capable of handling the photocurrent with a five order of magnitude variation is described. Transient simulation of the designed circuit shows that the output current takes 1.406ms to reach the steady state value, giving rise to a maximum speed of 0.7 frames per second for a  $1000 \times 1000$  pixels and 5.5 frames per second for a  $128 \times 128$  pixels. This design is appropriate for taking still pictures.

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